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Reconfigurable Neuromorphic Computing: Materials, Devices, and Integration

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Neuromorphic computing has been attracting ever-increasing attention due to superior energy efficiency, with great promise to promote the next wave of artificial general intelligence in the post-Moore era. Current approaches are, however, broadly designed for stationary and unitary assignments, thus encountering reluctant interconnections, power consumption, and data-intensive computing in that domain. Reconfigurable neuromorphic computing, an on-demand paradigm inspired by the inherent programmability of brain, can maximally reallocate finite resources to perform the proliferation of reproducibly brain-inspired functions, highlighting a disruptive framework for bridging the gap between different primitives. Although relevant research has flourished in diverse materials and devices with novel mechanisms and architectures, a precise overview remains blank and urgently desirable. Herein, the recent strides along this pursuit are systematically reviewed from material, device, and integration perspectives. At the material and device level, one comprehensively conclude the dominant mechanisms for reconfigurability, categorized into ion migration, carrier migration, phase transition, spintronics, and photonics. Integration-level developments for reconfigurable neuromorphic computing are also exhibited. Finally, a perspective on the future challenges for reconfigurable neuromorphic computing is discussed, definitely expanding its horizon for scientific communities.

1. Introduction

Artificial intelligence (AI) has the promise to provide human beings with a disruptive insight into every aspect of life, with applications ranging from face recognition,[1] medical diagnosis[2] to robot control.[3] However, conventional computing featured by centralized information processing suffers from the von Neumann bottleneck which brings about power-hungry and data-intensive computing, limiting the prosperity of AI.[4–6] Neuromorphic computing, as an emerging computation paradigm with distinguished brain-like characteristics, presents superiority in extremely high energy efficiency and intrinsic error tolerance.[7–18] Despite the prosperity of neuromorphic computing,[8,10–12,19–25] the customized schemes for dedicated stationary applications present a formidable challenge for tackling the dynamic data distributions in ever-changing scenarios and impair the model flexibility of biomimetic hardware. Most of existing neuromorphic devices cannot be reconfigured to fulfill the diverse run-time requirements, and hence depend on tailored designs specific to targeted applications.[26,27] For example, neurons for specific activation functions,[28,29] artificial dendrites,[30] and physical reservoir computing[31] are difficult to be reconfigured thus far which play a vital role in neuromorphic computing. Furthermore, energy- and area-efficient neuromorphic hardware imposes stringent requirements for the integration of multiple sophisticated brain-like functions in an all-in-one manner.[32–37]

Reconfigurable neuromorphic computing, an on-demand paradigm highlighting a disruptive framework for ultra-efficient artificial general intelligence, can maximally reallocate finite resources to perform the proliferation of reproducibly brain-inspired functions, bridging the gap between different neuromorphic implementations. For instance, different kinds of artificial neural network (ANN) architectures or brain-inspired computing primitives could be constructed by expanding the diversity of field-effect characteristics in a single semiconductor junction device,[38–41] further contributing to the customer-oriented versatility. Having these reconfigurable capabilities in neuromorphic hardware is of critical importance for future AI applications to be equipped with powerful potency by increasing functionality instead of complexity. Reconfigurable capabilities of neuromorphic hardware can be comprehended from the four aspects:

- Supporting for diverse dynamically customized functions: The reconfigurable neuromorphic devices are designed for higher integration of various on-demand computing paradigms in an

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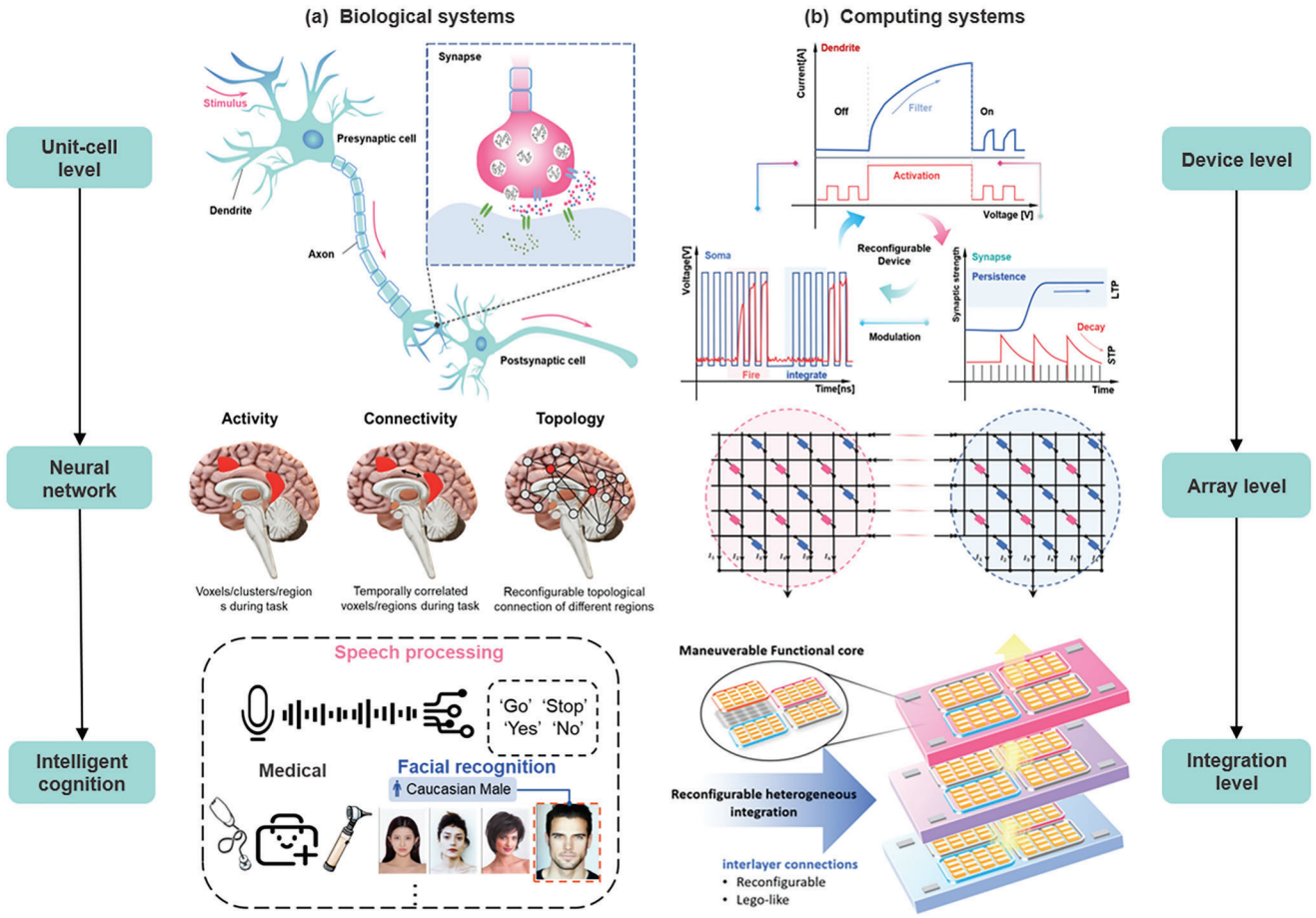

Figure 1. Biological and computational reconfigurability. a) Inherent reconfigurability of the brain with three hierarchical architectures, namely, unit cells, neural network topology, and intelligent cognition. b) The hierarchy of the reconfigurable neuromorphic computing at the three progressive levels inspired by the human brain, namely, device, array, and integration level. The miscellaneous reconfigurability of neuromorphic hardware platform can be provided by material engineering, device configuration, array topology, heterogeneous integration, and so on.

all-in-one manner. For example, synaptic short-term plasticity (STP), long-term plasticity (LTP), dendritic integrate-and-filter ability, or somatic integrate-and-fire function can be integrated in one device cooperating with simplified circuits, consequently contributing to the summation of originally separate practical applications.[38,39,42–44] It can support for self-adaptive dynamic functions within a single device, an approach that requires much fewer devices and power in comparison with static counterparts, and therefore achieves a high system complexity and computing performance.

- Supporting for the reproducible switch: The switch between different modalities should be noninvasive and reversible so as to ensure execution of multifunction with high endurance.
- Maximized reutilization of finite hardware resources: Reconfigurable hardware platforms enable to personalize hardware modules in a limited timescale overcoming intricate microfabrication of dedicated schemes, which significantly enhance the degree of miniaturization and intelligence and improve cost efficiency for a certain design.
- Higher universality and portability: One of the major pursuits of reconfigurable neuromorphic computing is excellent universality and portability, which endows the devices to be rearranged and assembled as general building blocks in different types of ANN architectures.

In the past decades, tremendous efforts have been made to pursuit reconfigurability of neuromorphic computing. Here we pick some representative works as listed in **Table 1**.

Specifically, compared to conventional static computing, reconfigurable neuromorphic computing paradigms, motivated by the inherent programmability of biological neural networks for fickle circumstances, can be further interpreted from material, device, and integration level (**Figure 1**a,b). Novel materials such as organic materials,[43,51,69–71] low-dimensional semiconducting materials,[72–74] superconducting materials[75–77] offer an attractive platform for modulating abundant neuromorphic responses and promise to provide brain-inspired devices with unprecedented tunability, high-speed and low-energy performance. At the device level, a single device could be repurposed by simple external signals to present switchable functionalities of neurons, synapses, dendrites, and so on.[38,39,42–44] Correspondingly, the bio-membrane potential can be dynamically reshaped by external stimulus (e.g., ion concentrations and electrical current), and the ion channels on the membrane serve as reprogrammable

Table 1. Summary of reconfigurable neuromorphic computing using emerging devices.

Principle	Material	Reconfigurable functionality	Switching voltages/field	Endurance	Retention	Power consumption	On-Off ratio	Feature size	Time scale (Switching)	Reference
Cation migration	MoO_x/Cesium Halides	Synaptic plasticity & multiple logics	$< 0.18\ V$	$> 10^5$	$> 10^6 s$	3.3 –37.5*aJ*	$> 10^{10}$	$< 5 \times 10^{-4}\ mm^2$	$< 200\ ns$	[45]
	$CsPbBr_3$	Threshold, binary, analog switching	$\leq 1\ V$	5.6×10^3 -2×10^6	$10^5 s$	$\approx fJ$	$\geq 10^3$	$\approx 300 \times 300 nm^2$	$< 23\ ms$	[46]
Anion migration	SnO_x/MoS_2	Tunable stochastic dynamics	$\approx 1\ V$	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*	$\leq 2s$	[47]
	TiO_2	Synaptic plasticity & multiple logic	$30\ V$	8.3×10^3	10*years*	0.147*fJ*	10^5	$\approx 100 nm^2$	$\approx 42 ns$	[48]
EC Doping	WO_3/phosphosilicate glass/Pd	Multiple synaptic weights covering a 20× dynamic range	$\approx 10\ V$	10^5	$\approx 100 s$	$\approx 10\ fJ$	*N/A*	$\approx 100 nm^2$	5*ns*	[49,50]
	PEDOT: PSS	>500 reproducible synaptic weights	$\approx 1\ V$	*N/A*	25*h*	$< 10\ pJ$	*N/A*	$10^3 \mu m^2$	$\approx 10 ms$	[51]
	PCPDTBT-SO_3K	Dual modes for logics(e.g.,and, nor, or, and nand)	$0.3\ V$	*N/A*	*N/A*	*N/A*	*N/A*	$\approx 100 \mu m^2$	$\approx 1 ms$	[52]
	H-doped $NdNiO_3$	Spiking neurons, synapses, resistors, capacitors	$0.45\ V\,\mu m^{-1}$	1.6×10^6	$10^5 s$	$\approx 2\ fJ$	6	$\approx 100 \mu m^2$	$1\ ms$	[39]
Ferroelectric	Ag/PZT/Nb: $SrTiO_3$	256 synaptic weights	$\approx 10\ V$	$> 10^9$	$10^4 s$	$5.3\ fJ$	≈ 200	$1.5 \times 1.5 \mu m^2$	$300\ ps$	[53]
	α-In_2Se_3	Heterosynaptic plasticity and Boolean logic	$\approx 4\ V$	10^3	2 *days*	$\approx pJ$	10^3	$5 \times 5 \mu m^2$	$\approx 100 ms$	[54]
	HfO_2	Neuronal functionalities & plasticity	$< 2.2\ V$	$> 10^4$	*N/A*	*N/A*	10^5	$30 \times 80 nm^2$	$\approx 1 \mu s$	[55]
Phase Change	$Ge_2Sb_2Te_5$	IF neuron and STDP synapses	$\approx 1\ V$	*N/A*	*N/A*	$< 100 \mu W$	*N/A*	$\approx 90 \times 90 nm^2$	$\approx 100 ns$	[56]
MIT	NbO_2	15 different neuromorphic responses	$\approx 2\ V$	3×10^{11}	> 1 *hour*	$\approx 2 pJ$	*N/A*	$25 \times 25 nm^2$	$\approx 0.1 \mu s$	[57]
	$V/VO_x/HfWO_x/Pt$	Synaptic plasticity & neurons	$\approx 1\ V$	$RS > 10^{10}$ $TS > 10^{12}$	10^4 s	$\approx 0.1 pJ$	$> 10^3$	$\approx 1 \mu m^2$	$\approx 1 \mu s$	[58]
Superconductivity	$YBa_2Cu_3O_7$	IF neurons & synaptic network	$\approx 1\ \mu V$	*N/A*	*N/A*	$\approx 1 aJ$	*N/A*	$200 \times 200 \mu m^2$	$\approx 1 ns$	[59–61]
	Mn & Nb	Multiple synaptic plasticity	$\approx 1\ \mu V$	*N/A*	*N/A*	$\approx 3 aJ$	*N/A*	$\approx 10 \times 10 \mu m^2$	$\approx 10 ps$	[62]
Spintronics	CoFeB	Synaptic weights & activation function	$\approx 200 Oe$	*N/A*	< 10 *year*	$\leq 16 pJ$	*N/A*	$3 \mu m^2$	8*ns*	[63]
	Pt/Co/AlO_x	NAND, NOR, XOR & full adder	$1000 Oe$	*N/A*	*N/A*	$< 20 pJ$	*N/A*	$10 \times 10 nm^2$	$< 100 ps$	[64]
	$Ni_{81}Fe_{19}$	Reconfigurable training and reservoir computing	$\leq 300 Oe$	*Indefinite*	*Indefinite*	*N/A*	*N/A*	$\approx 200 \times 600 nm^2$	$\approx 260 ps$	[65–68]

resistors which facilitate the reconfigurable operations in initiation, processing, and transmission of information.[78,79] From array devices, the reconfigurable topologic connections of neuromorphic building blocks, such as memristive crossbar arrays, can be fashioned to provide multilevel neuromorphic order parameters or sustain numerous computing primitives.[34,35,80–82] Meanwhile, from the aspect of biologic neural networks, the frontal parietal lobe network, as the core cognitive functional engine in biological systems, can flexibly perform cross-paradigm integration by reconfiguring dynamic topology between forehead and the default areas, thus facilitating parallel execution of multiple cognitive assignments, such as episodic memory and attention.[83,84] At the integration level, reconfigurable heterogeneous fusion[14,36] and integration,[85,86] as well as many-core architecture[13,87–90] can also provide significant versatility. This kind of chip-level reconfigurability contributes to concurrent emulation of various biological cognitive systems, such as sensing-processing-cognition integration for speech identification, complex logic computing, in situ memory for face recognition, multifunctional intelligent medical diagnosis, and so on.[33,36,38,82,13,87–97]

Although reviews concerning neuromorphic computation have been provided,[4,9,21,98] most of them are always stuck on static implementations those execute specific functions in specific contexts. To the best of our knowledge, a comprehensive review about how to achieve dynamic reconfigurability on neuromorphic hardware platforms is yet lacking till now. Therefore, it is highly important to thoroughly summarize state-of-art progress about reconfigurable neuromorphic computing including materials, devices, and integration, which would function as a concise and comprehensive introduction for future investigation. We focus on the interaction between mechanism and response characteristics, as well as all-around conclusions of materials, device configurations, and integration technologies. Accordingly, we introduce the reconfigurable computing paradigms at the device and integration levels. Specifically, based on reprogrammable material properties and modulation mechanisms at the device level, we respectively explore the unique modulation properties of ion migration (Section 2), carrier migration (Section 3), phase transition (Section 4), spintronics (Section 5), and photonics (Section 6). Additionally, Section 7 describes emerging important advances in the development of reconfigurable neuromorphic hardware integration. Finally, a perspective on the future challenges for reconfigurable neuromorphic computing hardware is provided at the end of the review.

2. Ion Migration

As one of the most common and important operating principles for neuromorphic devices, ion migration has shown great potential in realizing the majority of important bio-mimetic neural functions.[99–101] The fundamental idea of ion migration is to elaborately control the ionic dynamics inside the material by means of external stimulus, for example, optical pulses[73,102–104] or electrical field,[49,51,52,99,105,106] and eventually achieve the variation in intrinsic properties of materials which can be easily measured, such as conductance. With an emphasis on the modulating mechanism, one could classify the ion-migration implementations into cation filament- (Subsection 2.1), anion migration- (Subsection 2.2), and electrochemical doping-based mechanisms (Subsection 2.3). In the following subsections, we first provide brief introductions on fundamental operation principles and respectively review the reconfigurable hardware implementations of neuromorphic computing in the corresponding parts.

2.1. Cation Migration

Cation migration-based devices, also known as electrochemical metallization (ECM) devices or conductive bridging devices, are major type of fundamental component used for reconfigurable neuromorphic hardware platform. Electrochemical metallization, especially the spatially separated oxidation and reduction of metal ions, is imperative for the formation of cationic filament. Simply triggered by electrical or optical stimulus, noninvasively reversible control can be executed in ECM devices and subsequently facilitates the reconfigurability in plenty of configurations and effective materials, such as MoS_2,[107–109] halide perovskite,[110,111] graphene,[74,112,113] and organic materials.[43,51,69–71] In this part, we begin with the fundamental physical structure and principles of ECM devices and then present the state-of-art progress on reconfigurable neuromorphic hardware implementations including hybrid neuronal and synaptic functions, multiple-plasticity functions, as well as reconfigurable logic functions.

ECM devices are typically composed of electrochemically active anode, electrochemically inert cathode, and a solid electrolyte thin film as shown in **Figure 2**a. The formation of filament (SET operation) can be divided into three steps: an anodic electrodissolution process under sufficient positive bias voltage, an electric field-driven cationic migration across the electrolyte, and an electrochemically reductive recrystallization on the cathode surface. For example, when a positive bias is applied to the active metal (M) electrode, the oxidation reaction of active metal happens, leading to the accumulation of M^+ cations at the interface. Under continuous voltage promotion, M^+ cations migrate toward the inert electrode. Subsequent reduction and recrystallization of M^+ into atom forms happen at the interface between the inert cathode and solid electrolyte, which will result in conductive bridges linking the different terminals of device. It should be noted that the oxidation and reduction processes occur in spatially different electrode-electrolyte interfaces, which ensure filament formation goes with a swing. Electrochemical redox-caused formation of metal filament brings about a short-circuiting low ohmic state which owns the nonvolatile property. Conversely, applying sufficient reverse-polarity voltage will induce the emergence of RESET operation owning to filament dissolutions, setting the device into a high resistive state.[21]

The major progresses of cation migration-based devices for reconfigurable neuromorphic computing have mainly concerned hybrid neuronal and synaptic functions, and in-memory logics, providing numerous opportunities in this field. Detail discussion on both topics is provided below.

2.1.1. Reconfigurable Dual Paradigm of Both Synaptic and Neuronal Functions

For ECM neuromorphic devices, one of the important investigations in reconfigurability is dual-paradigm switching of both

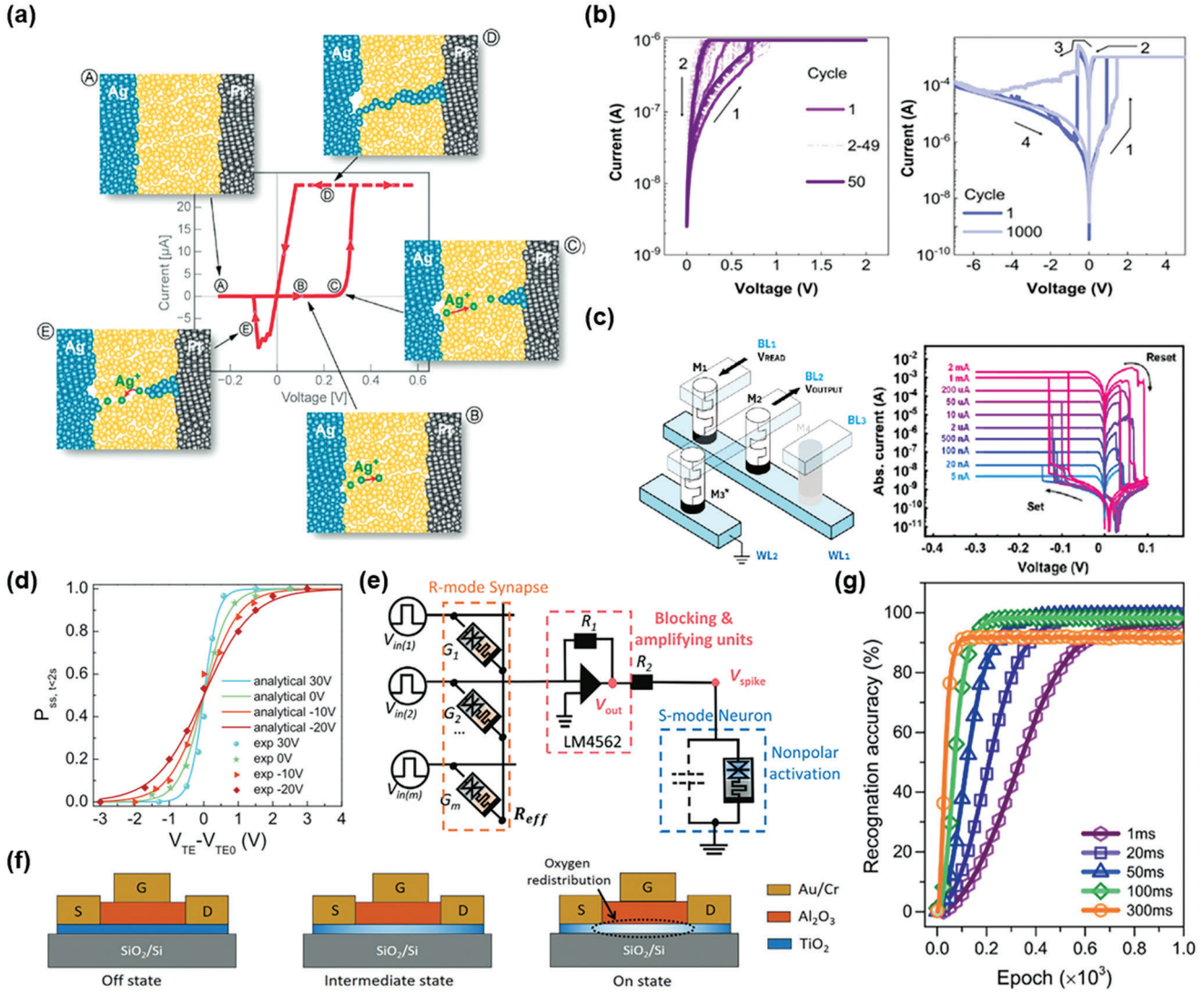

Figure 2. ECM-based reconfigurable neuromorphic devices. a) Fundamental operation principle of ECM cells. Reproduced under terms of the CC-BY license.[92] Copyright 2022, The Authors, published by IOP Publishing. b) Reconfigurable dual-paradigm switching between volatile diffusive mode (left) and nonvolatile drift mode (right) memristive characteristics upon applying DC sweeping voltages by modulating the ionic drift and diffusive mechanisms. Reproduced under terms of the CC-BY license.[110] Copyright 2022, The Authors, published by Springer Nature. c) The right one exhibits multilevel nonvolatile states achieved by ECM memristors. The left one refers to the reconfigurable logic-in-memory crossbar configuration made by four 1T1R ECM memory elements. Reproduced with permission.[45] Copyright 2022, American Chemical Society. d) Probability as a function of the bias voltage, presenting exponential-class sigmoidal distributions whose parameters can be dynamically reconfigured by gate voltage. Reproduced under terms of the CC-BY license.[47] Copyright 2021, The Authors, published by Springer Nature. e) Fully memristive neural network integrated by RRAM-mode synapses and selector-mode neurons. Reproduced with permission.[58] Copyright 2022, John Wiley and Sons. f) Schematic structure and operational principle of ultrafast resistive field effect transistor (ReFET) using proximity-oxidation-grown TiO_2 as the active channel. Reproduced with permission.[48] Copyright 2022, John Wiley and Sons. g) Image recognition accuracy for 5 different LTP/LTD optical pulse within 1000 training cycles. Reproduced with permission.[104] Copyright 2021, John Wiley and Sons.

neuronal and synaptic functions. In general, the emulation of neuronic leaky integrate-and-fire (LIF) functions can be realized by a volatile threshold switching (TS) mechanism, and biosynaptic characteristics are fashioned by nonvolatile resistive switching (RS).[110] Although exploring diverse mechanisms and materials accelerates the respective developments of artificial synapses and neurons, a significant issue urging one's concern is how to offer a viable unifying solution that can actively control over these two specifications when hindered by poor switching performance and unruly morphology of cation-filament devices. For this purpose, existing efforts mainly focus on modulating redox-state concentration or morphology of metal filament to achieve deeper reconfigurability of neural devices.[72,73,110,114]

By combining controllable ionic diffusion and drift mechanisms, John et al. demonstrated a reconfigurable memristor that portrays preferable manoeuvrable switching between synaptic nonvolatile mode and neuronal threshold mode by programmable ECM (Figure 2b).[110] This device consists of $CsPbBr_3$

nanocrystals with oleylguanidinium bromide ligands capped as an active switch matrix and can be controlled only through DC voltage without extra engineering. To be specific, reversible modulation of synaptic weight is guaranteed by stable filaments which are formed by the cation drift mechanism, and the low activation energy of Ag^+ and Br^- facilitates their diffusive migration that consequently contributes to volatile neuronal patterns. Compared to previous dual-paradigm memristors, excellent incorporation of perovskite and organic capping ligands gets rid of reluctant electroforming initialization and weakened retention, which further brings about low switching voltages (≤ 1 V), low currents (≤ 1 μA), and record-high endurance in both volatile (2×10^6 cycles) and non-volatile (5.6×10^3 cycles) modes. Furthermore, by utilizing 25 reconfigurable perovskite devices, a fully-memristive reservoir computing framework was qualified to process temporal signals and classify neural firing patterns.

In addition to drift and diffusion dynamics of ions, exploring novel electrolyte forms and architectures with low-dimensional material also enables preferable on-demand switching characteristics. By directly controlling the filamentary morphology through 1D material, Milano et al. proposed an all-in-one neuromorphic device by using single-crystal ZnO nanowires (NWs) as electrolytes.[72] Asymmetric-electrode configuration (Ag–Pt) effectively prevents NWs from overheating-induced breakdown. What's more, benefiting from Ag filament dynamic on NWs surface, reprogrammable multiple functions such as multistate nonvolatile bipolar switching, selector functions, and STP were successfully integrated into a single memristor, all of which promote the realization of self-assembled NMs-based artificial neural networks (ANNs).

Indirect control over the redox-state concentration with the aid of low-dimensional material has also present potential in reconfigurable modulation of filamentary dynamics. Zhou et al. introduced 0D bimetal gold–silver core-shell nanoparticles into the electrolyte which serve as discrete nucleation centers with excellent charge trapping and transport properties for regulating filaments.[115] This rationally-designed reproducible filament dynamics smoothly brought about reconfigurable bistable RS and multi-plasticity synaptic functions, such as paired-pulse depression (PPD), paired-pulse facilitation (PPF), post-tetanic potentiation (PTP), spike-time-dependent plasticity (STDP), as well as short-term to long term transition.

Reprogrammable band engineering has also shown significant reconfigurable implementations at both device and array level. Wang et al. demonstrated an Ag/(InP/ZnS) QDs/Indium tin oxide memristor with dual-mode switching through the noninvasive ultraviolet light programming operation.[73] Benefiting from the barrier effect of ZnS shell under ultraviolet light, the photoexcited-hole aggregated QDs accelerate the rate of modulating Ag^+ concentration, which accounts for the reversible transition from nonvolatile RS to volatile TS. Furthermore, a reprogrammable 9×9 visual data storage array and the LIF neuron were successfully achieved to meet the maneuverable application requirements of electronics in the future.

Apart from single redox mechanism, another thread is to employ competition between electrochemical migration and thermodynamic relaxation. Li et al. utilized above-mentioned effect to present novel filament modulation schemes of 1D Ag nanoclusters.[44] The Ag nanoclusters were introduced at the electrolyte/electrode interface and precisely controlled by external pulses that faithfully emulate biological Ca^{2+} motions. It is verified that the reconfigurable Ag nanocluster dynamics are dominated by electrochemical migration and thermodynamic relaxation, which facilitate the integration of neuronal spiking and synaptic functions (e.g., metaplasticity, asynchronous classical conditioning, and spike-timing-dependent plasticity, namely, STDP) in a single device, thus paving the way for on-demand unit-cell-level neuromorphic devices.

2.1.2. Reconfigurable In-Memory Logics and Neuromorphic Computing

Reconfigurable logic-in-memory architectures are beneficial for tackling data-intensive neuromorphic computing. Boolean logic operations can easily be performed by a single human neuron, which inspires artificial neuromorphic systems to develop diverse reconfigurable logic-in-memory computing with less hardware requirement than ever before.[116] Reconfigurable in-memory logics, on the other side, featuring binary computation, can be used to construct binary neural networks (BNNs), which might be a preferable cost-efficient scheme for executing deep learning than GPUs.[38,117]

It is worth noting that cation filament devices based on ECM have been proven feasible to achieve reconfigurable logic-in-memory functions which promise to be further utilized in brain-like computing. Recently, a reconfigurable conductive-bridging memristor with stable multilevel programming capabilities was qualified (Figure 2c), which can sustain reconfigurable complete Boolean functions and further multifunctional neuromorphic computing.[45] In this work, Cesium Halides are applied as a solid electrolyte for excellent on-off ratio (exceeding 10^{10}) and the incorporation of MoO_x interfacial layer in bottom electrode enables stable filament switching. The MoO_x layer effectively regulates the transformation of the conductive filaments (CFs) owing to its nonstoichiometric nature, thereby promoting the reliability and linearity of memristors with forming-free, ultralow operating voltage. The consequent low variation (< 30 mV) and high reproducibility ($> 10^5$ cycles) in a wide dynamic range have been favorably used to implement reconfigurable logic-in-memory functions based on a programmable 1T1R crossbar array configuration. By integrating the sensing ability, a reprogrammable optoelectronic memristor array was fabricated, using ITO as the bottom electrode, ZnO as the active layer, and Ag as a top electrode, to achieve sensing-memory-computing integrated paradigms, in which reconfigurable hybrid optical and electric modulation of fundamental neuromorphic parameters were verified.[118] Consequently, this memristor exhibits multiple nonvolatile biological functions with a higher dynamic regulation ratio of ≈ 25 than ever before, enabling array-level sensing-computing integrated Boolean logic operations with high reconfigurability. Furthermore, the memristor array-based face identification task was achieved by system-level integration of reconfigurable memristors array with an accuracy of 86.7%.

Compared with other redox-modulated devices, the energy-efficient property, superior scalability, changeable filament morphology, and a wide range of material choices combined with crossbar architecture endow the ECM devices with the

attractive potential for neuromorphic reconfigurability. Although substantial research efforts have been reported, the number of attainable synaptic nonvolatile states is limited, and emulation of neurons only focuses on LIF characteristics thus far. Moreover, application-level implementations of reprogrammable ECM neuromorphic devices, such as digital identification, are still in laboratory stage. Therefore, exploring richer neural dynamics and better endurable switching is necessary to meet deeper brain-inspired computing requirements.

2.2. Anion Migration

For devices based on anion migration, the change in material properties (e.g., conductivity) is induced by directed movement of anions such as oxygen ions, sulfur ions, and organic anions. Detailed investigations concerning the utilization of anion migration for reconfigurable neuromorphic devices have been amply implemented recently.[119] Herein, filamentary and non-filamentary types of anion migration-based devices are classified and summarized from the various reconfigurable neuromorphic aspects.

2.2.1. Filamentary Type

Typical anion migration-based filamentary devices usually demonstrate a metal/insulator/metal sandwich structure similar to ECM devices. Both of the metal electrodes in this kind of devices are inertial, while ECM devices require at least one active metal anode as just mentioned in Section 2.1.[120] When applying an appropriate voltage to the electrodes, the anions or vacancies in the insulator migrate, causing the formation and annihilation of conductive filaments, corresponding to various resistance states of the device.[121] The displayed nonvolatile resistive property of filamentary anion-migration electronics has been demonstrated desirable to implement memristive neuromorphic devices,[35,122–124] which allows for not only simulation of multi-plasticity synapses[58] and stochastic neurons[47] but also neural networks that can facilitate associative memory and hardware-based pattern-recognition task, at relatively high energy efficiency.[18,125]

Modulating fundamental neuromorphic parameters (e.g., synaptic weights) through resistive control constitutes a promising candidate for enhancing reconfigurability in neuromorphic electronics. Hu et al.[125] demonstrated both single- and multi-associative memory capability by constructing a memristive Hopfield network, which is implemented through HfO_2 memristive devices and peripheral circuits. The intrinsic reconfigurability of synaptic resistance matrix derives from the formation and destruction of oxygen vacancy-induced filaments, consequently bringing about diverse positive and negative weights. Utilizing elaborate adjustment of pulses, the resistive matrix of memristive Hopfield network can be fashioned and fixed into desired values, which further sustains the storage of multiple patterns for processing. Consequently, powerful associative memories are qualified feasible using this memristive Hopfield network and can achieve emulation of humans' "weak" and "strong" memories.

Motivated by inherent random movements of anion in filamentary dynamics, reconfigurable stochastic neurons equipped with controllable statistical behaviors have been favorably demonstrated utilizing memristive devices.[111,126] On account of SnO_x/MoS_2 heterogeneous memristive architecture, Yan et al. reported a probabilistic neuron to achieve dynamically tunable exponential-class sigmoidal distributions resembling physical Fermi–Dirac distribution (Figure 2d).[47] This three-terminal heterogeneous memristor accomplishes unprecedented accurate modulation of its statistic distribution simply through gate voltage that previous two-terminal counterparts disable to fulfill. The probabilistic statistic function with reinforced reconfigurability enables memristive neurons to execute the searching features of Boltzmann machines, further guaranteeing selected "cooling" strategies that can subsequently be used in maximum satisfiability problem.

Beyond above-mentioned partly memristive neuromorphic configurations, fully memristive neural network, as an advantageous post-complementary metal oxide semiconductor (post-CMOS) hardware paradigm, has unveiled prospects in implementing reconfigurable neuronal-synaptic-integrated functions by employing the synergistic effect of anion migration and other mechanisms.[58] Based on $V/VO_x/HfWO_x/Pt$, a memristor was demonstrated to obtain programmable dual modes by utilizing the coupling effect of $VO_x/HfWO_x$ functional layers, whose highly reproducible switching capabilities stem from the formation of anion filaments in Hf-doped layer. Anion migration in $HfWO_x$ contributes to realization of nonvolatile resistive properties for simulating bio-synapses, while the volatile neuronal selector mode derives from Mott transition in VO_x layer. The integration of dual functions in the same memristor not only significantly simplified the hardware configuration for synapses, but also achieved the twofold capacity of information encoding for neuronal functions than ever before, highlighting a cost-efficient pathway for hardware platforms of fully memristive neural networks, as shown in Figure 2e.

With the fundamental mechanisms based on anion filament, the well-performed emulation of synaptic and neuronal characteristics together with high reconfigurability among diverse brain-inspired functions, make these memristive devices promising competitors for neuromorphic computing. Notably, utilizing large-scale crossbar array configurations that equipped with above-mentioned memristors has been qualified as an up-and-coming approach to execute in-memory parallel computing paradigms. These crossbar array architectures fully take advantage of the abandonment of digital/anologue conversions, substantially decreasing the time loss and energy overhead, which highlights the potential of neuromorphic electronics for higher integration.[35,123,124]

2.2.2. Non-Filamentary Type

Although anion migration-based filamentary devices have been extensively studied for memristive neuromorphic implementations, the intrinsic stochastic dynamics, nonlinearity, and asymmetric variation of such filamentary electronics that arise from random kinetic displacement of anions significantly hampered the further accurate modulation and miniaturization.[124,127,128] As a preferable scheme than filamentary type, filament-free anion migration-based devices, featuring deterministic

switching that derives from dominant controllable statistic behaviors rather than atomic stochastic dynamics, enable ion migration-modulated electronics to work in a reproducible and energy-efficient manner.[129] How to achieve ultrafast operation speed and high energy efficiency are the two vital long-term goals those neuromorphic electronics long for. In this subsection, we discuss non-filamentary anion migration mechanism and the recent progress in implementing reconfigurable neuromorphic devices with high processing speed and low power consumption.

Ultrahigh operation speed promise to be actualized by reconfigurable in-memory neuromorphic paradigms on the basis of filament-free anion migration mechanism. Kumar et al. reported an ultra-speedy (≈ 42 ns) in-memory ReFET using proximity-oxidation-grown TiO_2 film as functional layer, whose fundamental mechanism attributes to redox-induced speedy redistribution of oxygen in TiO_2.[48] The accurate regulation of resistivity was simply realized by adjustable gate pulse and enabled the devices to perform reconfigurable in-memory logics through designed digital Boolean circuits. The intriguing reconfigurable characteristics of ReFET (Figure 2f) endow this in-memory device the abilities to implement neuromorphic computation such as synaptic multiplasticity, on-demand learning, and forgetting behavior, as well as pattern recognition. Notably, although this kind of filament-free schemes has present advantages such as excellent on/off ratio (10^5) and better retention (> 10 years) performance, the gate voltage for storage is up to 30 V in this work and how to achieve relatively low working voltage is still a problem of great concern, calling for further investigations.

Higher energy efficiency, as another long-term pursuit for large-scale neuromorphic computing, potential for runtime extension, stability enhancement, and cost reduction, have been successfully achieved in eco-friendly biomimicry visual systems by using photosensitive material. The reconfigurability stems from anion migration-based programmable photoresponse, showing profound implications for highly-integrated first-stage image processing.[43,102–104,130] Motivated by biological retina, in-sensor computing paradigms for image perception have been verified to be feasible through this mechanism, while how to achieve the excellent wavelength selectivity remains a key factor for future intelligent applications. By utilizing organic carbon nitride (C_3N_4) as the floating gate, Park et al. presented wavelength-selective photonic synaptic transistors,[103] which achieved biologically-comparable femtojoule-level energy consumption. Beyond this conventional visual system with relatively large power consumption and complex circuitry, self-powered progressive optoelectronic paradigms can offer a breakthrough for energy and computation efficiency. For instance, self-powered non-volatile optoelectronic synapses with programmable manifold memory ability and simplified circuitry were successfully demonstrated by Kumar et al.[130] Actuated by displacement of oxygen vacancies, the effective depletion width of NiO/TiO_2 heterojunctions can be elaborately modulated, which subsequently contributes to the multilevel nonvolatile voltage and photocurrent response. This reconfigurable electronic-photonic coupling effect further enabled this single photoactive heterostructure to simplify the amount of device terminal for flexibility and to mimic nearly all-around bio-characteristics of synapses, such as excitation or depression, manifold memory ability, PPF, and so on, where the training energy consumption was calculated down to 0.3 nJ per event. A small-scale array-level integration with these 5×5 two-terminal photosensors was implemented to qualify the classification of optical spatiotemporal information.

Although the above-realized optoelectronic processors have demonstrated the potential power in artificial visual systems for neuromorphic computation, latency, and hardware redundancy induced by the optical-electronic coupling interface hamper the speedup and high energy efficiency, which urge for the novel paradigms of hardware. Full-optically driven hardware platforms rendering ultrahigh computing speed promise to get rid of these shortages by unobstructed optical interconnection. Ahmed et al. introduced a reconfigurable field-effect phototransistor with excellent ultraviolet tunable photoresponse which can perform in-pixel information processing.[104] Based on multilayer 2D black phosphorus (BP), the natural oxide layers (P_xO_y) on both surfaces of BP induced in-gap defect states, elaborately controlling the trapping and detrapping of photoexcited carriers. This kind of surface-adsorbates defects that work as trapping centers helped to achieve wavelength-controlled multilevel conductivity through fully light modulation, acting as the cornerstone of device-level reconfigurability. The adopted fully-light approaches can achieve ultralow power consumption and ultrafast speed which is more than two order of magnitude shorter than state-of-art optoelectronic devices. To demonstrate the neuromorphic computing performance, supervised learning and facial recognition were successfully carried out by using this BP-based all-optical transistors for emulation of optical neural networks, which realize enhanced accuracy (> 90%) within 1000 training cycles (Figure 2g).

2.3. Electrochemical Doping

With elaborately designing the terminal configurations and electrolyte layers, the functional ions inside the electrolytes could be gently redistributed or migrate into channel material, resulting in the multilevel resistance change. In this subsection, we will introduce the recent achievements of reconfigurable neuromorphic computing from the perspectives of electrochemical (EC) doping mechanism, which utilizes gate-dri[1–4]ven migration of ions into channel materials for EC redox reactions and consequently induces the carriers' doping. By appropriately engineering the material and architecture of devices, EC doping can be manipulated at relatively low voltage, and the corresponding devices promise to relax the requirements for energy-efficient versatile brain-inspired applications.[131–133] Compared to other electrolyte-gated-based mechanisms (e.g., electric double layer), EC doping also induces a much higher on-off ratio and hysteresis degree, which is favorable for realizing neuromorphic reconfigurability.

Extraordinary-linearity EC doping-based synaptic transistors using ionic liquid and $SmNiO_3$ were introduced as early as 2014 by Shi et al. By designing appropriate channel and electrolyte materials,[134] EC doping has presented abilities of accurate modulation through a wide extent of oxidation and reduction states. However, on account of the unruly characteristics of liquid-electrolyte components, conventional EC transistor-based synapses suffer from unreliable LTP characteristics, low retention time, and ambiguous plasticity, which are greatly detrimental to the design of tunable multi-modal neuromorphic

devices.[135] Wang et al. demonstrated a multi-plasticity synaptic transistor with threefold tunable temporal properties based on the solid-state organic material system.[43] With the assistance of ferroelectric dipole switching, the EC synapses possess three on-demand plasticity including STP, minute-level LTP by EC doping, and extra 1000-second-persistent LTP by ferroelectric mechanism (**Figure 3**a). The reconfigurable switching of these working modes can be simply achieved by changing amplitude of applied gate voltages. Incorporating light-sensitive electronics, these artificial synapses facilitate an ultra-flexible light-triggered neuromorphic device with capabilities of addressing light intensity and frequency which have been utilized in primary visual-perception-recognition tasks.

Reconfigurable protonic resistors, as the vital building blocks in analog deep learning, are capable of executing intricate neuromorphic computation as demonstrated by Onen et al.[49,50] Their rationale for modulating neuromorphic state parameters is electrochemically tuned intercalation of the smallest and lightest ions, protons, into WO_3 channel to change the reconfigurable device conductance. Benefitting from the extremely electron-insulating property of nanoporous phosphosilicate glass (PSG) and noninvasive conduction of protons, these reprogrammable resistors enable ultrahigh pulsed electric field and consequently super-fast energy-efficient nanoionic devices, at least 10^4 times as speedily as biological synapses (Figure 3b, top figure). High endurance and extraordinary retention behavior (non-degrading operation over 10^5 pulse and 30 h) (Figure 3b, bottom figure) confirm the replicability of the device, promising to achieve further reconfigurability in analog deep learning whose ultra-high processing speed and far less energy consumption transcend its digital counterpart.

Apart from the inorganic material-based devices mentioned above, EC organic neuromorphic devices, which inherently possess dual-paradigm properties, have presented tantalizing opportunities to construct an attractive electronic platform for reconfigurable neuromorphic electronics owing to their facile and scalable printing characteristics. Organic neuromorphic devices could also present powerful potential in power efficiency, multi-functionality, and biocompatibility. Early in 2017, Burgt et al. qualified that EC neuromorphic organic devices based on poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS) film possess the ultrahigh density of non-volatile states (> 500 distinct states within a $\approx$ 1 V range) with excellent cycling performance and low energy consumption.[51] They also demonstrated the biocompatibility and mechanical flexibility of this organic device which highlights the potential of configuring versatile neuromorphic interconnecting platforms. Inspired by these distinct multilevel states of EC organic neuromorphic electronics, substantial efforts were made to demonstrate their dual-paradigm characteristics, such as volatile/nonvolatile and enhancement/depletion modes. Yu et al. proposed a volatile/nonvolatile bi-mode neuromorphic transistor by employing EC doping mechanism along with the formation of electrical double layers controlled by external voltages.[70] This bi-mode device presents additional third states with high classification accuracy that can be exploited to emulate bio-nociceptor with tunable sensitivity. However, although organic EC transistors can be executed in both enhancement and depletion mode, the static property of which is a huge impediment to realize highly switchable neuromorphic devices. Very recently, based on the EC doping mechanism, Nguyen-Dang et al. reported reconfigurable dual-paradigm transistors employing a self-doped conjugated polyelectrolyte as the functional layer (Figure 3c).[52] The reconfigurable modulation was accomplished by simply tuning the polarity of applied voltage, which originates from concurrent existence of anion doping and cation dedoping of active material. The resultant reprogrammable transistors were used to execute multiple dynamic Boolean logics, paving the way toward reconfigurable neuromorphic electronics, such as BNNs for deep learning.[38]

Exploiting hydrogen dopants as donors to induce electronic phase transitions would also lead to reprogrammable conductivity change by electrically modulating electrolyte's band architecture.[39] A reconfigurable neuromorphic hardware platform made from hydrogen-doped perovskite nickelate ($NdNiO_3$) was successfully implemented through voltage-controlled band engineering. By utilizing hydrogen doping, electrons are non-invasively donated into electrolyte to modify band structure so that the valance change of nickel ions can be subsequently introduced. The reconfigurable computing functionalities of neurons, synapses, and memory capacitors were successfully integrated into such a single device, whose run-time cross-modality switching is simply achieved by external voltage pulses (Figure 3d–g). All-around reconfiguration of brain-inspired functions were further qualified: the memory-capacitor mode was used for constructing the key elements of reservoir computing, and the obtained neuronic and synaptic modes were leveraged to configure the self-adaptive grow-when-required networks which can implement unsupervised learning for intelligent recognition.

3. Carrier Migration

Aside from ion dynamics, carrier migration as another indispensable operation principle has also been explored in neuromorphic applications. "Carrier migration" here only refers to the migration of electrons and holes, which can be modulated by electric field, optical or ferroelectric modulations. The adjustable and switchable carrier migration behaviors under various external stimuli can mimic biological neural functions, which offers promising prospects to implement reconfigurable neuromorphic hardware.[91,136] In this section, we review the recent advances of reconfigurable neuromorphic computing utilizing devices based on carrier migration by highlighting the modulation approaches containing electric modulation, optical modulation, and ferroelectric modulation.

3.1. Electric Modulation

Electric modulation (EM) is one of the vital candidates to efficiently regulate carrier migration by adjusting the amplitude and polarity of the applied voltages. EM has been extensively studied for carrier migration due to its better stability and faster response speed compared to counterparts based on other mechanisms, especially ion migration.[21] In this subsection, we mainly focus on different reconfigurable functions relying on the EM of carrier migration.

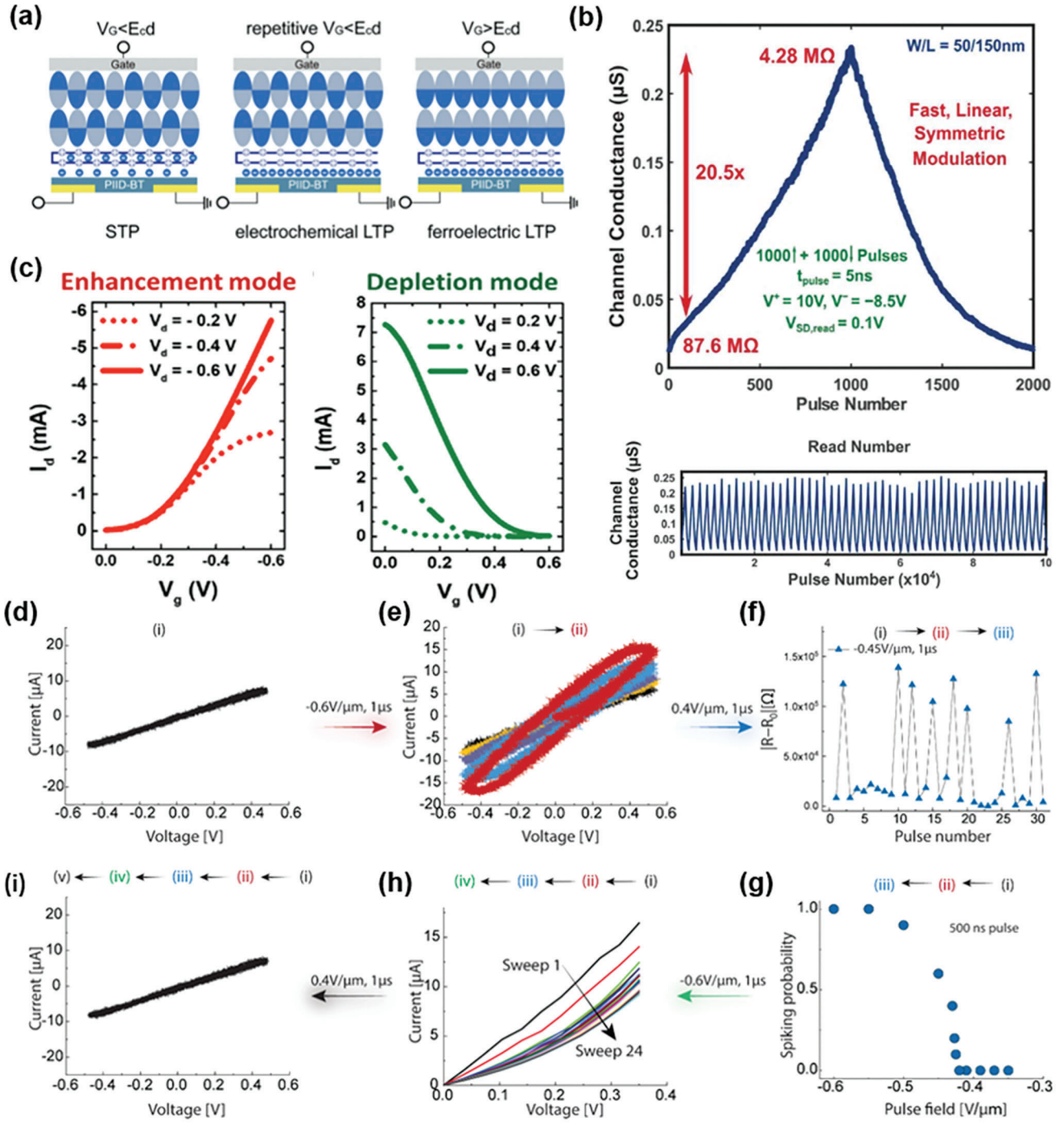

Figure 3. Electrolyte doping-based reconfigurable neuromorphic devices. a) Three reprogrammable plasticity: EC doping-induced STP (left) and LTP (middle), as well as ferroelectric LTP (right). Reproduced with permission.[43] Copyright 2018, John Wiley and Sons. b) Performance of ultrafast protonic reconfigurable resistors. The top and bottom panel shows the modulation and endurance performance, respectively. Reproduced with permission.[49] Copyright 2022, The American Association for the Advancement of Science. c) The dual modes of self-doped organic transistors. Left and right panel show the enhancement and depletion mode, respectively. Reproduced with permission.[52] Copyright 2022, John Wiley and Sons. d–i) Reconfigurable functions of a single perovskite device simply modulated by electrical pulse, including resistor (d,i), memcapacitor (e), neuron (f), stochastic behavior (g), and synapse (h). Reproduced with permission.[39] Copyright 2022, The American Association for the Advancement of Science.

Neuromorphic devices with electric field-controlled dynamic learning characteristics are conducive to realizing continuous learning in neural networks. Recently, Hersam et al. presented a reconfigurable memtransistor with monolayer MoS_2 that can be used for continuous learning in SNNs.[137] The Schottky barrier height at the source/drain electrodes changes with varying gate biases due to defect migration and charge trapping. Consequently, the memtransistor can realize tunable LTP and LTD, mimicking biological synaptic weight update and neuroplasticity. Benefiting from the gate-tunable synaptic properties, five learning curves can be realized via varying gate amplitude, which was further used to implement unsupervised continuous learning in simulated SNNs, demonstrating the flexibility to perform different tasks by dynamically reallocating the resource. However, the memtransistor exhibits nonlinear and asymmetric potentiation/depression, which is detrimental to effective network training. Notably, the situation can be changed by connecting two devices with opposite weights to cancel out the asymmetry or by optimizing programming pulses.[138,139]

Reconfigurable and bilingual (i.e., excitatory and inhibitory) synaptic devices are also concerned to provide several significant advantages, such as achieving higher similarity with biological synapse to simplify circuit design and preparation technology, toward more effective neuromorphic computing.[42,140] Motivated by the programmable electrically-doping properties of ambipolar materials, much progresses have been made in realizing reconfigurable synaptic hardware.[141,142] Ren et al. realized both excitatory and inhibitory synaptic behaviors in device based on twisted bilayer graphene with ambipolar conductance by tuning the bottom gate voltage.[143] Tian et al. designed a bilingual artificial synaptic device based on BP/SnSe heterojunction, the reconfigurability of which relies on electrical biases at presynaptic and postsynaptic terminal to implement excitatory and inhibitory paradigms. Superior STDP characteristics with better symmetry and higher synaptic weight changes were subsequently demonstrated.[144] Furthermore, to solve the problem that common synaptic devices need an additional terminal to realize heterosynaptic plasticity, Ding et al. presented a reconfigurable memtransistor using 2D WSe_2,[145] which can emulate both homosynaptic and heterosynaptic plasticity and achieve reconfigurable excitatory and inhibitory plasticity under the action of EM. Apart from synaptic multi-plasticity, other essential homosynaptic functions, such as spiking rate-dependent plasticity (SRDP), PPF, PPD, and filtering can be also achieved in this memtransistor.

Beyond ambipolar material-based schemes, combining p- and n-type semiconductors as stacked channels highlights a brand-new vista to implement reconfigurable bilingual synaptic functions. Very recently, Shim et al. proposed a stretchable device with bilingual synaptic behaviors,[42] by constructing a reconfigurable synaptic transistor with the bilayer semiconductor of n-type organic film, which adopts p-type single-walled carbon nanotubes (s-CNTs) networks as the stacked channel and a polyurethane (PU) elastomer as gate dielectric. Owning to voltage-induced different carriers and carrier migration directions, reconfigurable excitatory and inhibitory synaptic behaviors can be achieved (**Figure 4**a,b). The bilingual synaptic characteristic further enables the device to realize single- and dual-directional learning functions in neural networks. Based on the experimentally measured synaptic weight updates, a three-layer network is simulated with a recognition accuracy of over 90% for Mixed National Institute of Standards and Technology (MNIST) digits, even under 50% strain (Figure 4c).

Furthermore, many of attempts have realized the higher functional complexity by integrating reconfigurable synaptic and logic functions utilizing neural devices. Pan et al. demonstrated an electrically-modulated WSe_2 transistor, which can be employed for reconfigurable logic and neuromorphic systems.[38] Specifically, reversible electrical doping and carrier migration behaviors in the channel can be manipulated by dual gates and drain voltages, leading to various field-effect characteristics. Utilizing this switchable property, a logic cell with two WSe_2 transistors was designed to achieve multiple logic functions simultaneously. By further integrating three WSe_2 transistors and a capacitor, reconfigurable synaptic functions were proposed as shown in Figure 4d. The capacitor is utilized to modulate the potential difference across dual gates of device M1, the corresponding channel doping in device M1 allows the system to simulate synaptic excitation or inhibition by applying the pre- and post-synaptic spikes to devices M2 and M3, respectively. Besides, the system can achieve reconfigurable synaptic STDP by changing the relative potentials between V_1 and V_2 (Figure 4e,f), which requires fewer devices to achieve the same functions than MOSFET technology. Although the system can implement reconfigurable synaptic functions, the external capacitor limits its high-density integration. Scaling will require memory functionality which can be achieved by using ferroelectric or floating gate devices.[146–150] Xiong et al. introduced a reconfigurable logic-in-memory synapse based on BP/ReS_2 heterostructure.[151] By gradually tuning voltage pulses, they realized a nonvolatile ternary logic inverter that exhibits three distinct logic states, owing to the tunable carriers' trapping and de-trapping processes at the BP/ReS_2 interface. The BP/ReS_2 heterostructured device has a unique trilingual response property, that is, the synaptic weight change can be switched from inhibitory to excitatory and then back to inhibitory along with the gate voltage from −3 to 3 V. Besides, the ANN stimulation using the experimental data showcase recognition accuracies of ≈ 91.3% and 89.5% on small and large MNIST digits, respectively.

3.2. Optical Modulation

Compared with electrical modulation, the introduction of optical modulation endows neuromorphic devices with huge advantages such as high operation speed and ultralow power consumption. The exploration of synergistic photoresponse from specific junctions between various materials has also brought opportunities to demonstrate diverse functions of optoelectronic neuromorphic devices. Notably, optoelectronic neuromorphic devices are generally capable of optical sensing and information processing. Therefore, in addition to the regular synaptic plasticity and logic functions, they also show great potential in artificial vision systems.

In recent years, great efforts have been made to explore synaptic plasticity and logic operations based on optical stimuli.[152–154] A meaningful strategy is to design band alignment between heterojunctions. For example, Zhou et al. developed a Type-

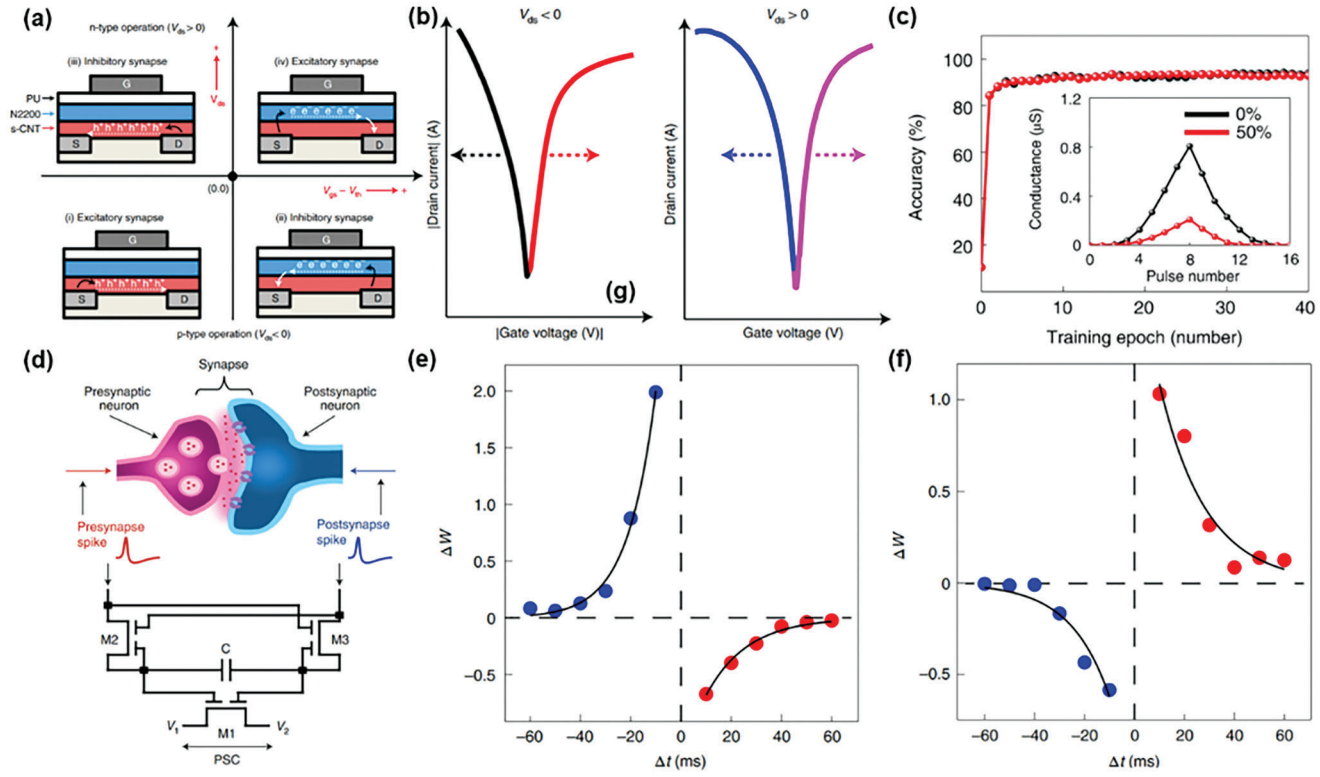

Figure 4. Reconfigurable neuromorphic devices based on purely electric modulation. a) Working mechanism of stretchable reconfigurable synaptic transistor. b) The transfer curves with inhibitory and excitatory synaptic responses under different operation circumstances. c) Backpropagation training results of dual-directional image recognition. Reproduced with permission.[42] Copyright 2022, Springer Nature. d) The illustration of biologic synapse (top) and implemented reconfigurable synaptic functions circuit (bottom). e,f) Reconfigurable synaptic anti-Hebbian (e) and Hebbian (f) STDP learning rule, which are achieved via changing the relative potentials between V_1 and V_2. Reproduced with permission.[38] Copyright 2020, Springer Nature.

II heterojunction based on MoS_2/PTCDA that allows efficient charge transfer at the interface of the heterostructure under laser pulse.[133] The device is capable of achieving optical synaptic excitatory and demonstrates a maximum long-term synaptic weight change of 60 which outperforms previous research based on optical modulation.[155–158] Very recently, Yang et al. reported a floating-gate transistor based on MoS_2/h-BN/graphene heterostructure, which demonstrates voltage-assisted light programming/erasing operation.[159] Thanks to this voltage-assisted bidirectional optical control, synaptic behaviors including LTP and LTD, as well as four reconfigurable logic gate functions (AND, OR, NAND, and NOR) are successfully implemented.

Despite different stimulation sources, the basic principles of synaptic function are universal in electrical and optoelectronic neuromorphic devices. It is therefore expected to achieve bidirectional updating of synaptic weights by pure optical modulation. Several all-optically modulated neuromorphic devices with maneuverable synaptic or logic functionalities were proposed based on materials, such as ZnO/PbS heterostructure,[160] perovskite/ZnO heterostructure,[161] and $PtSe_{2-x}$ films.[162] The utilization of defects is regarded as a promising strategy to explore bidirectional optical modulation. Ahmed et al. presented a fully light-controlled versatile synaptic device with defective BP.[104,163,164] The trap sites induced by natural oxide P_xO_y layer and surface adsorbates can act as scattering centers, thus negative photocurrent can be observed by applying 365 nm illumination. While being exposed to 280 nm wavelength light, the positive photocurrent generated because of the passivation of oxygen sites and the introduction of carriers. Such bipolarity photoresponse characteristics enable the BP device to mimic excitatory and inhibitory synaptic behaviors and achieve reconfigurable Boolean logic operations including nonlinear XOR gate. Though this study presents a potential for neuromorphic computation, the use of ultraviolet light would restrict artificial vision applications and cost more compared with visible light.

By considering the synergistic photoresponse of different materials, some neuromorphic devices based on hybrid structure have also successfully achieved bidirectional optical modulation and involve wavelengths in the visible range. In 2020, Lai et al. proposed an artificial synapse made of a Bi_2O_2Se/graphene hybrid structure with positive and negative photoresponses under illumination of 635 and 365 nm light sources, respectively.[165] Bidirectional synaptic characteristics and reprogrammable logic functions (AND and OR) were realized successfully in this device. Later in 2021, Hou et al. demonstrated an optical synapse based on pyrenyl graphdiyne (Pyr-GDY)/graphene/PbS QDs heterostructure which can implement bidirectional synaptic functions and more reconfigurable logic functions by 450 and 980 nm excitation (**Figure 5**a).[166] In detail, when exposed to 450 nm illumination, the photogenerated holes trapped in Pyr-GDY are a lot more than the photogenerated electrons trapped in PbS QDs, resulting in a net positive photogating effect and con-

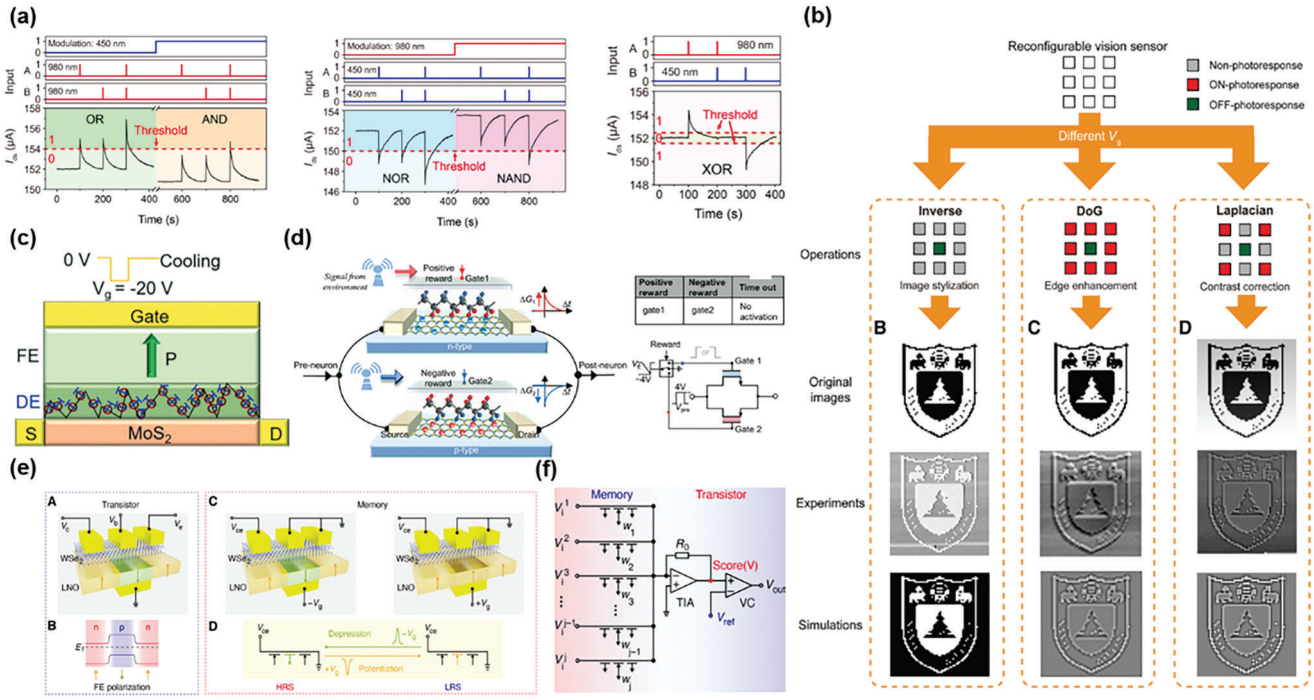

Figure 5. Reconfigurable neuromorphic devices based on optical and ferroelectric modulation. a) "OR", "AND", "NOR", "NAND", and "XOR" logic functions realized by using 980 and 450 nm optical pulses as input and modulatory input. Reproduced with permission.[166] Copyright 2021, American Chemical Society. b) Reconfigurable image processing realized by varying V_g. Reproduced with permission.[169] Copyright 2021, The American Association for the Advancement of Science. c) Schematic diagram showing the pinning of ferroelectric domain walls with oxygen vacancies and the resulting equivalent dielectric (DE) layer under the control of bias. Reproduced with permission.[172] Copyright 2022, John Wiley and Sons. d) Schematic illustration showing the update of synaptic weights with positive and negative reward, as well as the corresponding circuit diagram. Reproduced with permission.[173] Copyright 2022, John Wiley and Sons. e) Schematic diagram showing the reconfigurable functionality of basic device. The left part denotes nonlinear transistor functionality with the channel-polarity regulation of FE polarization. The right part denotes memory functionality with tunable resistance controlled by polarization reversal under positive and negative gate voltages. f) Schematic of the circuit diagram, where the memory cells and amplifier were integrated to realize binary classification. Reproduced with permission.[147] Copyright 2021, The American Association for the Advancement of Science.

sequent negative photoresponse. Instead, under illumination of 980 nm light, most of the light is absorbed by PbS QDs. The photogenerated electron trapped in PbS QDs would lead to a positive photoresponse. The bidirectional photoresponse feature endows the device with reconfigurable synaptic excitation and inhibition and five various logic functions including AND, OR, NAND, NOR, and XOR. Utilizing the linear and symmetric synaptic updates, the simulated ANN demonstrates an accuracy of ≈90% on MNIST digits. Furthermore, an integrated sensing-memory-processing system was demonstrated which can achieve real-time detection, in situ image storage, and processing, showing huge possibilities for future neuromorphic visual applications.

Based on the tunable photoresponse achieved by voltage-assisted or all-optical modulation, and in conjunction with the potential of optoelectronic devices in the field of artificial vision, several studies have begun to focus on how to further extend the reconfigurable device properties to application level. For instance, Mueller at al. developed a neuromorphic image sensor based on a reconfigurable WSe_2 optoelectronic device array, which can simultaneously sense and process images projected onto the array, overcoming the obstacles of the traditional separation modules.[167] Utilizing split-gate electrodes to electrically dope the channel, tunable responsivity of each pixel in the sensor can be formed. Based on this adjustable property, a classifier and an autoencoder were demonstrated, which are trained by supervised and unsupervised learning, respectively. Remarkably, the sensor can classify patterns correctly within ≈50 ns, showing exciting possibilities for future ultrafast machine vision applications. However, the experimentally demonstrated vision sensor lacks the ability to store the weights of the ANN, which would restrict its scalability. Apart from integrated sensing and processing functions, some efforts have realized all-in-one sensing, memory, and processing capabilities in emerging vision sensors, which offer tremendous potential for various applications, such as intelligent Internet of Things, autonomous vehicles, human-eye biomimetic vision, etc.[37,168] Wang et al. presented a reconfigurable neuromorphic vision sensor based on WSe_2/h-BN/Al_2O_3 heterostructure devices.[169] The devices can exhibit positive and negative photoresponse under light illumination at zero and negative V_g, respectively, which are attributed to the photoconductive effect and the defect-induced gate electric field screening effect. The photoresponsivity with opposite polarity endows the devices to simulate the biological characteristics of human retinal cells. Then, a reconfigurable retinomorphic vision sensor was implemented by connecting 13 heterostructure devices into an array. As shown in Figure 5b, by controlling these devices with indi-

vidual gate voltages, switchable image sensing and processing functionalities including image stylization, edge enhancement, and contrast correction were simultaneously realized. Besides, the sensor can work as a convolutional neural network (CNN) and perform image classification, which exhibits an accuracy of 100% with < 10 epochs when recognizing three various types of letters. Very recently, Hong et al. reported an ultrasensitive vision sensor with 2D perovskite-gated AlGaN/GaN phototransistors to demonstrate similar functions.[170] Owing to the photo-enhanced field-effect mechanism from the 2D perovskite, switchable positive and negative photoresponse can be realized in the phototransistors under different gate voltages, where bidirectional synaptic functions are successfully emulated. Moreover, a neuromorphic vision sensor based on 3 × 3 phototransistor array was constructed, which is capable of achieving three reprogrammable image preprocessing operations (Reverse, OFF-RF, and Embossing) by changing the applied gate voltages to each pixel and shows an accuracy of ≈100% when recognizing three letters with three colors.

In addition to reconfigurable image processing functions, neuromorphic vision sensors have also been demonstrated for polarization-perceptual applications by Xie et al. who proposed a neuro-transistor based on 2D ReS_2.[168] Utilizing the strong in-plane anisotropy of ReS_2, the neuro-transistor exhibits intriguing polarization-sensitive properties under polarized-light stimuli. The relationship between optical excitatory postsynaptic current and polarization angle varies with polarization wavelength, thus showing reconfigurable anisotropic vision. Besides, the neuro-transistor is capable of realizing reconfigurable polarized filtering functions, including low-pass, band-stop, and high-pass filtering. This result gives inspiration to researchers on how to develop applications by incorporating intrinsic properties of materials in addition to conventional visual sensor and opens more possibilities in the direction of neuromorphic devices with optical modulation.

3.3. Ferroelectric Gating

Compared with the traditional electrostatic gate, the ferroelectric gate is a more desirable approach to reversibly regulating the channel carriers by switching the up and down polarization directions in ferroelectric.[38,41,171] The polarization direction is correlated with the formation or depletion of the inversion layer in the channel, thus affecting the nonvolatile shift of the threshold voltage and program of multiple channel conduction states. Here, we highlight the material- and device-level achievements of ferroelectric field-effect transistor (FeFET) in recent years, where desired reconfigurable properties in specific neuromorphic applications are discussed.

Inorganic ferroelectric oxides are the mainstream type of gate material in FeFET. Despite the substantial development of ferroelectric oxides so far, several challenges that will affect the polarization effect still need to pay attention to.[174,175] It is conventionally believed that interfacial influences such as impurity adsorption, traps, etc. will enhance the depolarization effect, thereby weakening the regulation. A promising avenue to overcome this challenge lies in artificial design regulation. Gao and coworkers intentionally introduced the interfacial states on the ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ thin film during the annealing process, where different annealing parameters such as temperature and duration allow for conscious control of the density of surface states.[176] Combining the effect of ferroelectric polarization and interfacial charge trapping, the resulting $MoTe_2$-based FeFET performs a more stable switching behavior with reconfigurable synaptic functions. The back-gate current and drain current corresponding to the presynaptic and postsynaptic signals can be used to learn both STP and LTP by changing the number or frequency of V_g. To further enhance the understanding and development of the joint mechanism, Sun et al. proved a new principle for the $Bi_4Ti_3O_{12}$-MoS_2 device whose architecture can switch from a ferroelectric-semiconductor structure to a ferroelectric-insulator–semiconductor structure.[172] Both ferroelectricity and oxygen vacancies are fundamental requirements to achieve such reconfigurability, where the strong domain-wall pinning of oxygen vacancies contributes to the formation of insulator as shown in Figure 5c. The dominant mechanism transits from charge dynamics to ferroelectric polarization with the electric-filed-driven migration of oxygen vacancies. Apart from the polarization-dominant long-term memory, the device can be reconfigured as short-term memory with the synergistic effect of charge and ferroelectric polarization. Synaptic learning rules including STP and LTP with excellent linearity were achieved in a memory configuration, coupled with the low-power transistor configuration, showing strong potential for neuromorphic computing by memory-transistor integration.

Besides the synapses, the ferroelectric-oxide devices are also investigated to simulate the neurons, which is another fundamental component of brain-inspired neural networks. In 2018, Mulaosmanovic et al. utilized HfO_2-based FeFET to mimic pivotal neuronal dynamics.[55] By applying identical gate pulses below the threshold voltage repeatedly, the device transitions from OFF to ON, mimicking the integration of synaptic inputs of neurons. Apart from the LIF behavior, a tailored negative reset pulse is used to emulate the refractory period. Based on such simulation capabilities, reconfigurability of synaptic and neuronal functions was actually achieved. It is undeniable that achieving more perfect neuron behavior with purely ferroelectric devices requires more subtle design and deeper understanding, but this study undoubtedly presents huge possibilities for the future where ferroelectric neurons and synapses can construct all-ferroelectric neural networks.

Ferroelectric polymers are another attractive gate material in FeFET that has been extensively studied due to their indispensable merits including low-cost fabrication and excellent physical and chemical stability.[177] Based on the coupling between ferroelectric materials and channel semiconductors, areas with n- or p-type doping can be controlled to construct p–n junction. The effective and controllable doping capacity of organic ferroelectric polymers has been demonstrated in some research. For example, Zhai et al. reported the fine pn doping in MoS_2 by local patterned ferroelectric polarization of organic P(VDF-TrFE) polymer through the tip of atomic force microscopy in 2019.[149] Optoelectronic devices with switchable structures including p–n diode and high gain p–n–p bipolar transistor were successfully defined. Subsequently, arbitrarily altering the polarity of $MoTe_2$ was demonstrated using this ferroelectric polymer, and a variety of memory devices were constructed.[178] Therefore,

the universality of this doping strategy was confirmed, showing great potential for realizing different functional devices required in neuromorphic computing with limited hardware resources. From the perspective of neuromorphic applications, an inspiring study was proposed by Miao and co-workers who had already demonstrated that programmable doping can be realized in graphene channels.[179] In their latest research, by connecting two synaptic transistors composed of WSe_2 channel and P(VDF-TrFE) ferroelectric gate in a parallel structure, they found that the polarization-dependent channels can be tuned as one n-type and one p-type, corresponding to opposite synaptic weight update behaviors.[173] As illustrated in Figure 5d, when a positive (negative) reward signal comes, only the gate1 (2)-controlled channel is selected, thus increasing (decreasing) the total synaptic weight. Thanks to this opposite plasticity, a kind of reward-modulated STDP can be achieved, making the reconfigurable polarity a powerful strategy to realize the training of SNN for reinforcement learning with the much-simplified circuit.

In addition to FeFET where substantial research efforts have been dedicated, some other architectures based on ferroelectric were also proposed for further expansion in neuromorphic computing with reconfigurable devices or functions. Tong et al., in a bid to address the problem of lack of homogeneous devices in neuromorphic hardware where peripheral circuits and memories are always necessary but physically separated, proposed a WSe_2-on-$LiNbO_3$ architecture with reconfigurable functionality at the device level as shown in Figure 5e.[147] The effect of ferroelectric polarization on channels is equivalent to that of electrical doping, and therefore it is reasonable to construct p–n diodes and p–n–p bipolar junction transistors (BJTs) with the same device by the noninvasive control of the ferroelectric gate. Moreover, the polarization modulation of the ferroelectric domain can affect the built-in potential in BJT, further improving the on/off ratio of non-volatile memory. Multiple BJTs were cascaded to construct the operational amplifier with the realization of signal rectification, amplification, and voltage comparison. Since the operational amplifier used in the peripheral circuits and memory cells can be realized by the same device architecture, they directly achieved neuromorphic hardware that can be utilized for binary classification based on the homogeneous devices (Figure 5f), showing important academic significance and application prospects for promoting the industrialization and application of new neuromorphic hardware.

4. Phase Transition

In a broad sense, phase transition is the transition of a system from one steady state to another under the control of external parameters. Along with the reversible transition, significant changes in the physical properties of the system can be realized such as electrical resistance, photoresponsivity, thermal conductivity, and refractive index. This inherent variability of phase transition materials brings about various approaches to drive the phase transition, including temperature, strain, and electric field, providing abundant degrees of freedom to regulate the function of the phase transition device, which show great potential for the reconfigurable functionality. According to the mechanisms of phase engineering,[101,180] the effect of ferroelectric polarization, crystalline-amorphous phase change, metal-to-insulator transition (MIT), and superconductivity on reconfigurability in neuromorphic computing are reviewed in this section.

4.1. Ferroelectric Tunnel Junction and Ferroelectric Diode

In recent years, ferroelectric devices as typical nonvolatile memory have been intensively studied due to their permanent and switchable electrical polarization.[171,181,182] Switching the polarization direction of ferroelectric domains has emerged as a powerful tool for changing resistance according to the purpose, thereby showing the potential for utilization in reprogramming neuromorphic devices. To unveil the detailed mechanisms, as a representative device, ferroelectric tunnel junction (FTJ) with nanometer-thick ferroelectric layer sandwiched between two electrodes is selected for the full discussion. In addition, ferroelectric diode (FD) with ferroelectric semiconductor as the channel but without gate control also brings a new approach to the regulation of ferroelectric devices. For FTJ, the relationship between tunneling electroresistance and ferroelectric polarization can be revealed by considering the electron tunneling across the ferroelectric layer and the screening of polarization bound charges. Therefore, FTJ devices exhibit polarization-dependent tunneling current. Recently, by applying voltage pulses to the device, junction resistance can be continuously tuned to multilevel intermediate states, thus simulating the function of reconfigurable synaptic cells. As another basic but crucial biological property, STDP has also been demonstrated in FTJ devices (**Figure 6**a), exhibiting the potential capabilities of FTJ for brain-inspired computational architectures.

With the general goal of utilizing more states, many useful methods have been explored from both theoretical and experimental perspectives. Recently, Garcia et al. constructed a detailed model to predict the synaptic behavior and learning rule of FTJ.[183] Based on the direct relationship between the normalized reversed area and junction resistance, the change of resistance can be modeled by nucleation-dominated dynamics as a function of the voltage pulse. This theoretical model is essential for the design of reliable and predictable devices, paving the way for the customization of FTJ. Since then, researchers have begun to further refine the reprogramming capability of FTJ synapses including more distinguishable states and faster switching speed. Based on an Ag/$BaTiO_3$ (BTO)/Nb:SrTiO (NSTO) junction,[184] Li et al. investigated the close relationship between device performance and Schottky barrier, through modulating Nb-doping concentration and the work function of the metal electrode. With increasing Nb concentration, Schottky barrier height becomes lower, and more voltage drops on BTO barrier, thereby simplifying the pulse conditions required for polarization reversal. With the combination of optimal Nb concentration and Ag electrode with lower work function, the resulted device shows 32 nonvolatile resistive states under sub-nanosecond pulses (≈ 600 ps). As an encouraging result, the achieved ultrafast synapse facilitates the mass data processing, and demonstrates the practical potential of ANN simulation with high recognition accuracy (> 90%) on MNIST digits. An improvement scheme from the perspective of ferroelectric material selection was also proposed in their subsequent research,[53] in which (111)-oriented $PbZr_{0.52}Ti_{0.48}O_3$ (PZT) rather than traditional (001)-oriented PZT

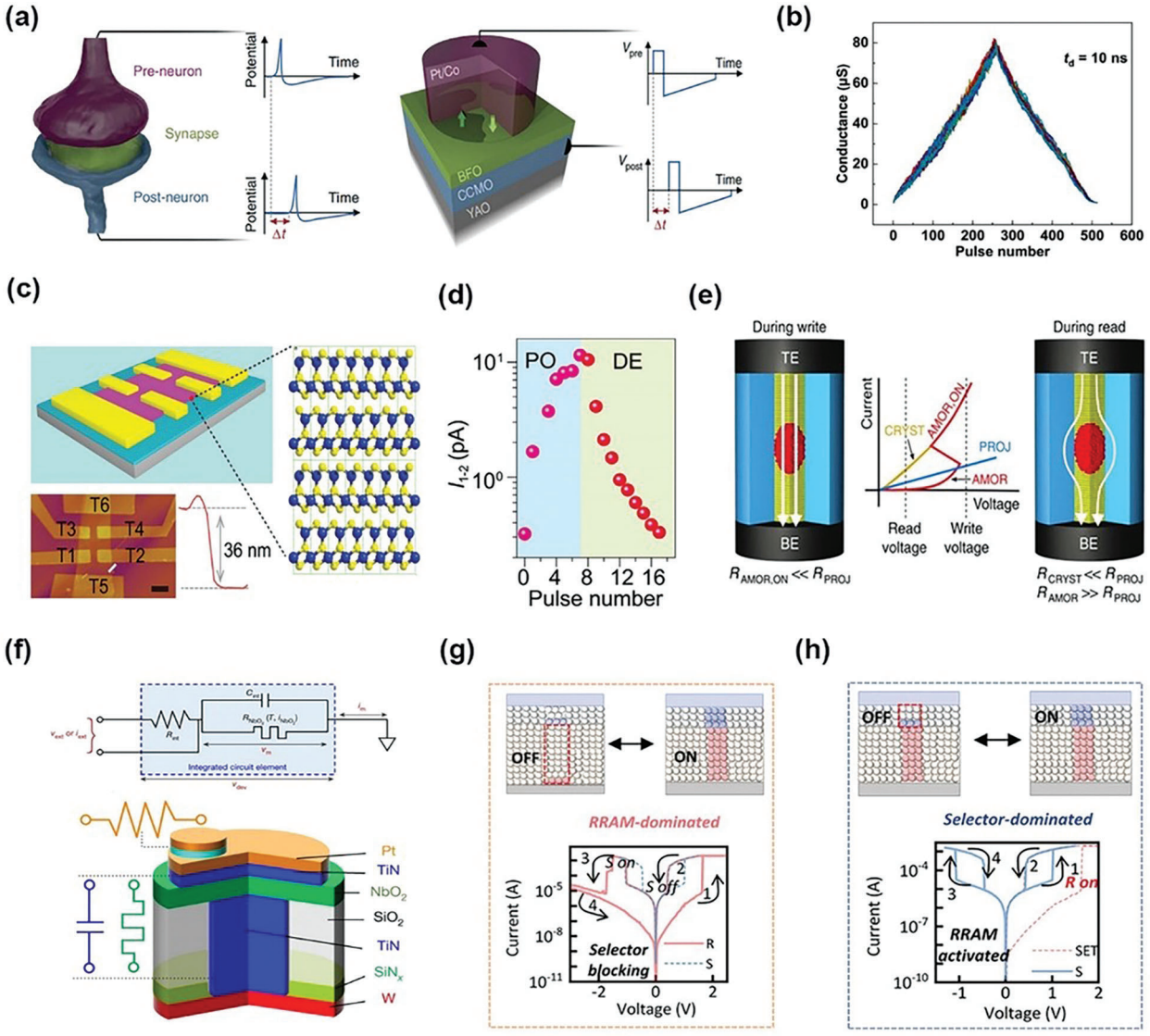

Figure 6. Reconfigurable neuromorphic devices based on various phase transition mechanism. a) Schematic diagram of pre- and post-neurons connected by synapse and the ferroelectric memristor. Reproduced under terms of the CC-BY license.[183] Copyright 2017, published by Springer Nature. b) Potentiation and depression processes. Reproduced under terms of the CC-BY license.[53] Copyright 2022, published by Springer Nature. c) Schematic diagram of the α-In_2Se_3 six-terminal memristor. d) The relationship between postsynaptic current I_{12} and pulse stimulation from T_6. Reproduced under terms of the CC-BY license.[54] Copyright 2021, John Wiley and Sons. e) Schematic diagram of projected phase change memory. Reproduced under terms of the CC-BY license.[193] Copyright 2015, published by Springer Nature. f) Circuit model and schematic diagram of the third-order electronic element. Reproduced with permission.[57] Copyright 2020, Springer Nature. g) Resistive switching of RRAM-dominated mode under a large sweeping voltage. h) Threshold switching of selector-dominated mode under a small sweeping voltage. Reproduced with permission.[58] Copyright 2022, John Wiley and Sons.

was explored to induce two-step switching dynamics, conducive to multilevel and stable intermediate ferroelectric domain states. As shown in Figure 6b, using the variable voltage scheme with 10 ns pulse width, the artificial synapse analog in the form of potentiation and depression presents remarkable linearity with 8-bit (256) conductance states. Particularly, this FTJ also achieves sub-nanosecond switching speeds (≈ 630 ps) at low voltages (< 5 V), as well as fast speed of 300 ps at higher voltages, showing substantial potential for low energy consumption. Owing to these outstanding performances, the simulated CNN can achieve a high recognition accuracy of 94.7%. The STDP rule is also demonstrated, opening enormous opportunities for the development of hardware synapses for on-demand customized applications.

In addition to traditional ferroelectric insulators, the research on novel ferroelectric semiconductors has become much more in-depth in recent years, thus paving the way for the development of FD.[185,186] The current switching in a FD should be dominated by the modulation of polarization charges on the Schottky barrier at the metal/semiconductor interface. Notably,

α-In_2Se_3, as a special ferroelectric semiconductor, has attracted much attention due to its simultaneous in-plane and out-of-plane ferroelectricity.[187] The former in-plane ferroelectricity provides a way to realize multi-terminal regulation through simple electrode configurations.[188,189] As can be seen from Figure 6c, Xue and coworkers demonstrated the polarization reversal of ferroelectric α-In_2Se_3 channel induced by multiple terminal inputs.[54] This in-plane resistance characteristic can be simply understood as the result of polarization modulation on the Schottky barrier at the metal/semiconductor interface. The third terminal of memristors can also realize nonvolatile control on the current flowing through the first and second terminals and obtain an excellent modulating effect with a record switching ratio over 10^3. Here, apart from inherent homosynaptic plasticity, heterosynaptic learning was also successfully emulated (Figure 6d), which means this multiterminal planar memristor can implement reconfigurable behavior of different kinds of synapses. The α-In_2Se_3-based neutral networks can further realize high recognition accuracy in supervised and unsupervised learning manners. What's more, without changing the architecture of the device, the planar memristor can naturally achieve Boolean logic functions including OR and NOR. In short, a single α-In_2Se_3 memristor is capable of realizing the functions of homosynaptic learning, heterosynaptic learning, and logic operations, which provides fundamental insights into energy-efficient and brain-inspired computing systems with simple structures.

The performance of devices modulated by ferroelectric polarization can also be qualified by multilevel nonvolatile photoresponses, which further expands reusability of ferroelectric-modulated devices. For instance, Liu et al. designed a special kind of ferroelectric photosensor with a simple two-terminal structure of Pt/$Pb(Zr_{0.2}Ti_{0.8})O_3$/SRO, where the ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$ layer endows the photosensor with reconfigurable photoresponse.[190] By applying different voltage pulses to set the ferroelectric layer in distinguishable polarization states before measuring the photocurrent, the polarization-modulated photovoltaic behavior was carefully investigated. The resulting photocurrent is in good consistency with the voltage pulse, which means both positive and negative photoresponse can be realized at the same device. Notably, this one-to-one correspondence feature for positive and negative weights will be critical for network construction with less hardware quantity. Inspired by the excellent synaptic behavior and switchable photoresponsivity of ferroelectric photosensor, they further built the ferroelectric photosensor network to implement the in-sensor MAC function (a simultaneous image sensing-processing operation), as well as deeper applications including pattern classification and edge detection. This achievement demonstrates the integrated sensing-memory-computing paradigms of ferroelectric neuromorphic devices, providing even more new concepts for real-time machine vision in the future.

As an emerging building block of neuromorphic computing paradigm, ferroelectric has attracted much attention due to its distinctive properties arising from inherent switching of spontaneous polarization and nondestructive electrical control methods, such as fast switching speed, multilevel intermediate states, and large OFF/ON ratio. Considerable research efforts have been devoted to demonstrating that inherent polarization reversal can provide a great convenience for reconfigurable neuromorphic applications mainly focused on the mimicking of synaptic cells. With the understanding of microscopic ferroelectricity, optimization of synaptic reconfigurability has been executed to pursue endurable switching with more distinguishable multilevel states, better linearity, greater variation range, and lower power consumption. Despite tremendous advances, further investigation and understanding are needed to break through current limitations. Some new concepts, such as the utilization of ferroelectricity based on the change of ferroelectric domain walls with nanometer thick rather than domains, can be seen as novel promising gateway toward brain-inspired neuromorphic computing. Whether based on this novel mechanism or the familiar domain mechanism, precise control, new measurement approaches, mature process fabrication, and advanced integration technology are urgently required to satisfy the demands of neuromorphic computing in the future.

4.2. Amorphous-Crystalline Phase Change

Amorphous-crystalline phase change materials (PCMs), a special class of materials characterized by their speedy transition between the crystalline phase and amorphous phase accompanied by changes in electrical and optical properties, are regarded as a strong contender for a variety of neuro-inspired applications.[191,192] In this subsection, we begin with the fundamental physical properties and principles of amorphous-crystalline phase change materials and then discuss the recent progress from the perspective of reconfigurability concentrating on neuromorphic synaptic and neuronic devices.

In the typical amorphous-crystalline phase-change devices, phase-change material is commonly sandwiched between two electrodes. The reversible resistance change between amorphous and crystalline states is widely utilized to store information.[193] The majority of the research in this area is based on $Ge_2Sb_2Te_5$ (GST) and other materials in the Ge–Sb–Te ternary phase diagram.[192] These PCMs remain amorphous under ambient conditions while behave like fragile glass at elevated temperatures. When the temperature is close to the transition temperature, the glass state crystallizes rapidly, manifesting as an abrupt resistance drop in electrical properties. This heating process for neuromorphic phase change devices is usually brought out by Joule heat from electric and laser stimulation. A long and low pulse, raising the temperature of the initial amorphous phase over transition temperature while below the melting temperature, is used as the SET operation. The corresponding RESET pulse is short in time while high enough to raise the temperature of crystalline phase over melting temperature, thus making PCM amorphous again.

For phase change devices, a typical reconfigurable application in neuromorphic networks is the emulation of weight update. In addition to the two basic states of amorphous and crystalline phases, more intermediate states can be realized by adjusting the ratio of amorphous and crystalline phases. Although the tunable multilevel states those can emulate the weight of the biological synapses were fully proven,[194,195] an issue still needed to be investigated and addressed is how to realize more stable intermediate states when constrained by rapid phase change with

spontaneous structural relaxation and inevitable thermal disturbances. To this end, several methods including designing the pulse shape,[196] optimizing the device structures,[197] and doping in PCM[198] to improve thermal stability were proposed and demonstrated. As early as 2012, Kuzum and coworkers designed a device structure comprising a bottom electrode with a small contact area and a top electrode like a mushroom to realize partial reset.[199] The resulting multistate phase change devices were utilized to simulate synaptic behavior and learn the rule of STDP, showing the ability to adjust the time constant and implement different STDP kernels. Then, a projected phase change memory was proposed as a solution for resistance drift and noise in 2015.[193] The projection segment decouple the storage and retrieval task (Figure 6e) and can be further designed to realize spatial geometric variations. Apart from removing these harmful impacts, another thread is to make use of the resistance drift effect to improve the precision of neural network and realize required stochasticity. A case in point was proposed by Shi et al. with the classification precision promoted to 93.2% from 89.6% after the introduction of the resistance drift effect, demonstrating the advantages of spontaneous synaptic weight modification.[200] Inspired by these improvements, the phase change synapses demonstrate their potential in several SNN applications and keep developing rapidly.

Another significant aspect of reconfigurability of phase change devices is the construction of all-memristive neuromorphic network, where switchable architectures between neurons and synapses are needed.[191] The membrane potential of neurons can be mimicked by the accumulation of electrical pulses in PCM, while the firing occurs when the conductance reaches the threshold. Subsequently, with a high but short pulse, the PCM returns to the amorphous phase and the current exhibits cut-off. Based on GST, Pantazi et al. experimentally demonstrated the versatile architecture for synapse and neuron based on the mechanism introduced above.[56] This neuromorphic architecture also can be used for unsupervised learning to learn multiple correlations, showing great practicability of PCM for all-memristive neuro-synaptic implementations.

Notably, the innovation of PCM-based neuromorphic electronics is always motivated by further understanding of the mechanism with focus on the design of the heaters, current path, and the improvement of materials. In the long term, such forward-looking guidance is generic and will continue to guide researchers in the expansion of PCM applications. Due to intrinsic thermally driven phase change, PCM inevitably suffers from some stability effects, however, as mentioned above, various approaches have been investigated to address or exploit these characteristics. Foreseeably, with the further refinement of the control methods, the phase change of PCM can occur in a smaller area and at a faster rate, enhancing the number of distinct synaptic states and energy efficiency, which is urgently needed for next-generation neuromorphic computing.

4.3. Metal-To-Insulator Transition

Metal-to-insulator transition (MIT) materials exhibit unusual insulating property that the insulated state can transform to the conductive state with drastic changes in electric, magnetic, optical, and mechanical properties when stimulated by some external conditions. Although the physical mechanisms of MIT materials require further investigation and understanding, several works have demonstrated their potential as reconfigurable cells in neuromorphic computing.

Here, we place emphasis on Mott MIT memory, the transition of which is derived from electron-electron interaction. When applying thermal energy, electric fields, and optical stimuli to Mott memory, electron localization occurs and the memory converts to a high conductance state. As has been extensively studied, Mott MIT memory is a typical volatile device. When the external signal is removed, the memory returns to a low conductance state again. This intrinsic reversible transition in the form of threshold switching (TS) provides tremendous support for simulating neuronal behavior and forming brain-inspired systems. The threshold-dependent current opening behavior corresponds to the LIF model of neurons, while the sharp current reduction after the withdrawal of external signals can satisfy the need for the refractory period of neurons.

A meaningful achievement based on NbO_2 volatile Mott memristor was under the spotlight for the realization of the programmable isolated third-order element. As shown in Figure 6f, each isolated element is composed of a memristor, a parallel capacitor, and a series resistor, possessing three state variables related to temperature, voltage, and transition dynamics.[57] By adjusting the applied voltage, different parts of its current–voltage curve can be selected on demand to perform specific output characteristics. As the voltage increases, the output characteristics can be summarized as sinusoidal oscillations, two-spike bursting, periodic single spikes, and damped spikes, realizing a total of 15 neuromorphic phenomena including LIF and refractory period adaptation by a single element. Based on these reconfigurable output characteristics, an integrated array was constructed to experimentally demonstrate analogue computing, further verifying the complex computing capabilities of this system are similar to thalamocortical computing in the brain. This work fully realized and explored third-order devices both theoretically and experimentally, opening a new avenue for compact functional neuromorphic computing.

Apart from NbO_2, another classic kind of MIT material is vanadium oxide. Although the debate on the driving mechanism of vanadium oxide represented by vanadium dioxide (VO_2) has not yet reached a clear conclusion, a generally accepted view nowadays is that a coupling of Mott transition and Peierls transition may exist in the VO_2. For brevity, we still discuss it as Mott material in a broad sense. Plenty of research has confirmed its application of neuron function simulation in SNN and deeply studied the influence of the frequency and amplitude of the input signals on triggering spike output signals. On this basis, a more ideal innovation is to realize switchable volatile and nonvolatile memory in VO_x, thus providing the possibility to build the synapse and neuron on the same device. Recently, Miao et al. designed multi-mode $V/VO_x/HfWO_x/Pt$ memristors to construct fully memristive SNN, in which the $HfWO_x$ layer represents nonvolatile RS due to oxygen vacancy migration while the VO_x is a TS layer.[58] By changing the dominant mechanism between RS and TS with different sweeping voltage, RRAM

and selector mode can be realized. Compared with TS layer, the thicker RS layer needs higher operating voltages. Therefore, a large sweeping range from −3 to 3 V corresponds to synaptic function based on RRAM-mode as shown in Figure 6g. On the other hand, by presetting the RRAM layer to the high conductive state and applying a small sweeping voltage from −1.2 to 1.2 V to the device, the selector mode is selected (Figure 6h) and the neural events can be emulated without any extra capacitor. Combining these two modes of devices, synapse-neuron integration was realized, and a spiking CNN was constructed at the level of networks to manifest the potential of these reconfigurable multifunctional devices in tackling the dataset learning task.

To sum up, we highlight two major advances in reconfigurable MIT-based devices for emerging neuromorphic computing. One emphasizes increasing the order of a single device, that is, the complexity, in order to achieve more kinds of neuron behaviors, thus improving the reconfigurability of the simulation function by an isolated hardware element. The other is summarized from the perspective of the dominant mechanism. The regulation of device mechanism realizes the volatile–nonvolatile switching, thereby manifesting the reconfigurability of fundamental neuromorphic components by construction of the isomorphic devices for synaptic and neuronic simulation. A common point is that these two achievements are not purely using MIT materials, but also the coupling effect of different materials, whether it is from the perspective of enriching the modulation mechanism, or for the sake of replacing peripheral electronic components. Collaborative efforts including an in-depth understanding of MIT dynamics, selection of materials for which the phase transition conditions are easy to implement, as well as development of characterization approaches and integrated technologies will foster the growth of this field.

4.4. Superconductivity

Although biologically inspired computing has shown extraordinary potential power in promoting the popularity of artificial intelligence and machine learning algorithms owing to its highly parallel computing paradigms with intrinsic fault tolerance and flexibility, conventional training platforms based on digital-logic optimization schemes have encountered unwilling difficulties like out-of-control energy consumption and associated memory bottleneck. Digital superconducting systems, as a promising post-CMOS concept, employing cryoelectronic device technologies, have shown significant improvements in neuromorphic computing for both energy-efficient and speed-up purposes.[201–207]

Josephson junctions (JJs)[59,61,62,75,208–210] and superconducting nanowires[211–214] are the two principal forces that directly access neuromorphic computing at the device level, with particular implementations often exactly dual with each other.[77] For instance, the ion channel dynamics of LIF neurons can be efficiently mimicked by two cascading JJs, and the emulation of neuronic relaxation oscillation can be realized by a nanowire resistor incorporation as well. In this subsection, we mainly focus on superconducting JJs and nanowires, which are two main up-and-coming candidates for realizing the reconfigurable biomimetic functions of neural networks.

4.4.1. Josephson Junctions

JJs are sandwich architectures with two superconductors separated by a nanoscale non-superconducting barrier for weak link coupling, promising diverse biological primitives at the single-device level which derive from DC Josephson effect or AC Josephson effect. Up until picometer-level focused helium ion beam fabrication technology has been successfully employed by Cybart et al. in 2015,[75] the direct manufacture of the insulated tunnel barriers of JJs is achievable above liquid-nitrogen temperature. In special, this kind of modern focused ion beam technology promises to construct planar JJs in a more reproducible and scalable manner, thus endowing the JJs intrinsic relaxation oscillations and spiking characteristics for neural functionality at the unit-cell level. Besides, JJs can also be viewed as flux-quanta valves which are vital elements for single-flux-quanta logical circuits.[201] Significant efforts on neuromorphic applications of JJs have popped up since then.

The hybrid modality of both synapses and neurons in a single device is one of the important goals for pursuing versatile reconfigurable neuromorphic hardware platforms. By using JJs design, Goteti et al. proposed a spiking recurrent neural network that features switchable collective response behaviors for both synapses and neurons.[59,61] Based on superconductors and Mott-insulating oxides, they employed a disordered array of JJ loops that can be modulated by the dynamics of light ions and geometric asymmetry (**Figure 7**a). The flux quanta migration in the disordered system (e.g., propagation through JJs and storage in superconducting loops with the form of circulating supercurrents) with intricate reconfigurable energy landscapes is qualified as the solid theoretical foundation for spiking behaviors of neurons and synapses at the device level. First, dynamic threshold modulation of LIF neuron can be achieved by configuring the junction critical current. The JJ critical current can be flexibly varied through the adjustment of loop size and geometry of focused He-ion tunnel barrier (e.g., varying the dose of injected ion damage). When changing the DC input, the threshold of neurons is correspondingly reconfigured so that the distinctive kinds of neurons can be dynamically defined.[59,60] Second, vortex dynamics, which can be reprogrammed by differing geometric configurations of this disordered array, result in exponential multiplicity of nonvolatile synaptic weights and subsequently enable synaptic learning behavior (Figure 7b). The synaptic weight-updating principle solely depends on electrically configuring the relative frequency and amplitude of the input and feedback currents rather than individual parameters. In their relevant work, these superconducting recurrent neural networks, in the form of highly compatible functional combinations of synapses and neurons, are capable of being reconfigured to execute both supervised and unsupervised learning.[61] Notably, the proposed superconducting schemes achieve extraordinary operating speeds up to a few terahertz as well as superior energy efficiency in the order of atto Joules per spike.

JJs can also incorporate with neuromorphic spintronics to achieve a novel reconfigurable implementation of ultralow-energy artificial intelligence schemes. Schneider et al.

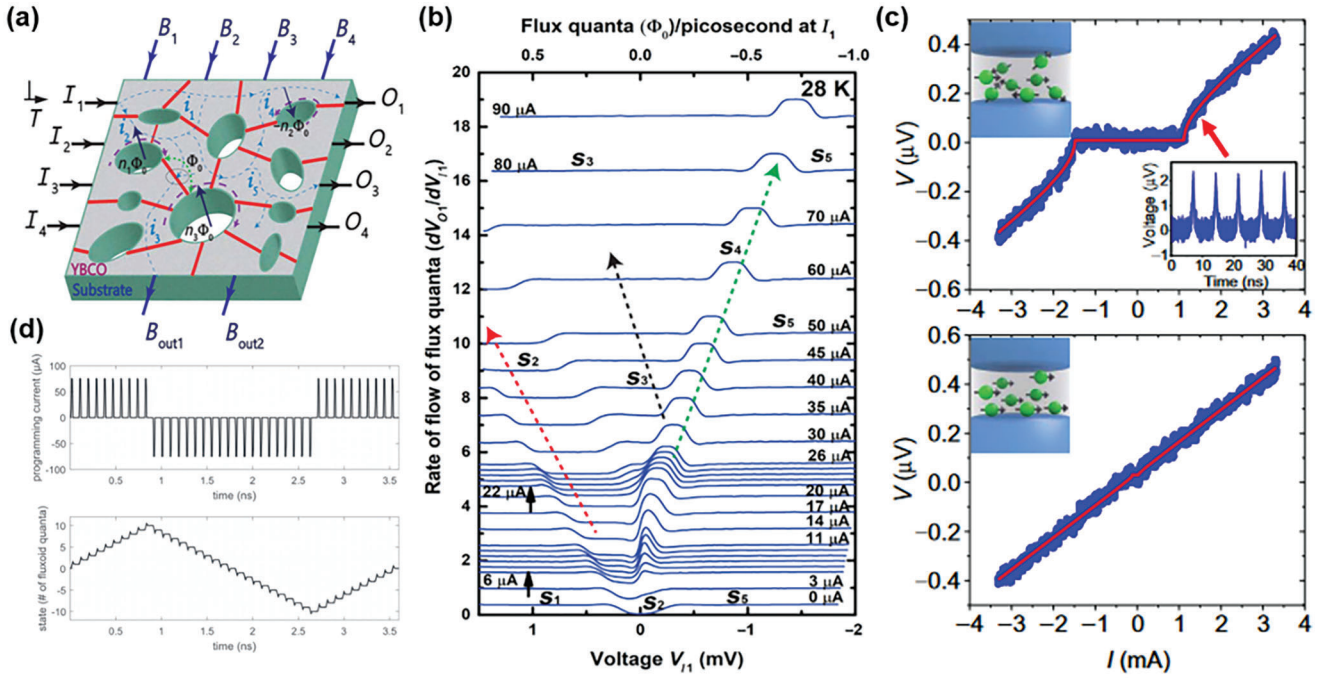

Figure 7. Superconductive mechanisms based reconfigurable neuromorphic electronics. a) Schematic of superconducting disordered spiking recurrent neural networks with superconducting JJs. b) Evolution of synaptic states represented by different rates of flux flow. Reproduced with permission.[61] Copyright 2022, The American Association for the Advancement of Science. c) Spin-dependent superconducting transport. Voltage–current characteristics of JJ synapse in the magnetic disordered state (Top) and magnetic ordered state (Down). Reproduced with permission.[62] Copyright 2022, The American Association for the Advancement of Science. d) 33 discrete reconfigurable states with symmetric switching properties which can be used for DNN accelerators. Reproduced with permission.[213] Copyright 2020, IOP Publishing.

demonstrated neuromorphic computing with JJs and spintronic nanoclusters, emulating artificial synapses with faster operation and energy-efficient performance (Figure 7c).[62] The dynamically reconfigurable JJs, consisting of silicon barriers containing spintronic manganese nanoclusters and superconducting Nb electrodes, have been used as the key elements of the artificial synapses. The researchers implemented artificial synapses through field-free analog modulation of JJ critical current. Under the influence of sub-attojoule electrical pulses, numerous magnetic nanocluster configurations were dynamically programmed, whose order is regarded as a function of the superconducting critical current. Consequently, by changing superconducting current, the reconfigurable upgradation of synaptic weight was qualified with a dynamic time scale exceeding 100 GHz and energy consumption down to 3 aJ. Furthermore, the implementation of non-Hebbian learning by using such a reconfigurable JJ synapse was demonstrated, showing great potential of JJs to construct programmable neuromorphic devices.

Notably, the achieved neuromorphic superconducting electronics thus far have mostly relied on JJs, owning to their mature fabrication and preferable properties like ultrahigh modulation speeds and ultralow energy consumption (approximately on the order of aJ per synaptic event).[215] Although JJs possess significant advantages in superconducting neuromorphic computing, the state-of-art digital JJs remain at a relatively low integration density compared to von Nomanan architecture. Comprehensive works on JJs need to be done in the future, and alternative platforms such as nanowire-based devices offer a fresh perspective on reconfigurable neuromorphic developments.

4.4.2. Nanowires

Quasi-1D superconducting nanowires (NWs), whose width and thickness are comparable to or smaller than the Ginzburg–Landau coherence length ξ and magnetic penetration depth λ, respectively, own the intrinsic non-linearity and reconfigurable superconducting-normal switching controlled by the threshold current. Dominated by thermal dissipation and phase incoherence, NWs support gain improvement, high fanout, large impedances, and compatibility with complementary metal oxide semiconductor (CMOS), making them appealing to the hardware schemes of neuronal spiking events. For example, parallelly in cooperation with resistors, NWs are capable of producing relaxation oscillations that mimic collective neuronal behaviors. However, the oscillation frequency, dictated by the NWs' high kinetic inductance, is slower than that of JJs, consequently limiting switchable binary operations. Nevertheless, scalability, robustness in noisy circumstances, and fitness for fan-out make NWs continuously draw researchers' attention to neuromorphic computing such as deep neural networks[213] and spiking neural networks.[211,214]

Onen et al. present a unit-cell neuromorphic crosspoint device based on superconducting NWs, aiming at the acceleration of deep neural network trained by relieving hectic data transfer.[213] Benefiting from the inherent carriers' inertia of

superconductors, the enhanced kinetic inductance can be easily maintained which contributes to a higher number of reconfigurable non-volatile states. Based on the single-flux-quantum principle, the researchers were able to produce 33 reprogrammable states through applying narrow pulses, which are further utilized in performing analog multiplication (Figure 7d). The reconfigurability has been further guaranteed by the extraordinary symmetry characteristic of the non-volatile unit devices, deriving from the internal discretized nature of flux quantization which enables plenty of non-degraded cycling. These NW-based devices further being assembled in a crossbar array have been described for accelerating deep neural network training to implement the calculation of derivatives, with the aid of a back-propagation algorithm.

Apart from deep neural network accelerators, another emerging idea about superconductive NWs-based neuromorphic computing is to emulate the biorealistic spiking neural networks.[211,214] The sufficient employment of inherently coupled relaxation oscillations of NWs forms the cornerstone to simulate the essential behaviors of neurons, such as spiking and firing, and further can be utilized for mimicking small-scale spiking neural networks.[216] Although their negligible energy consumption and miniaturization highlight the potential for robust neuromorphic applications, superconducting NWs-based electronics still suffer from inconsequent switching and slow reset times which hinder their development a lot. Most importantly, how to achieve a deeper reconfiguration and larger scale of CMOS-compatible neural systems, is still difficult which appeals to more research efforts than ever before.

5. Spintronics

With distinguished properties such as stochastic function,[217–219] oscillatory,[220–222] low power consumption,[11,223] as well as non-volatility and plasticity,[65,224,225] spintronic devices have recently emerged as competitive candidate for neuromorphic computing, which is capable of transmitting information via the precise modulation of spin transfer torque (STT), spin orbit torques (SOT), as well as isolated magnetic textures (e.g., domain walls, skyrmions, artificial spin ice, and so on). These diverse approaches enable spintronics to be easily reconfigured in a more compact and energy-efficient manner.[65,226–230] Here, we will focus on magnetic tunnel junctions, spin orbit torques, domain walls, skyrmions, as well as artificial spin ice (ASI), and discuss their implementations in reconfigurable neuromorphic computing.

5.1. Magnetic Tunneling Junctions

Magnetic tunneling junction (MTJ) possesses appealing characteristics for brain-like computing such as extremely low read power consumption, non-volatility, distinguished read/write endurance, high-speed voltage operation, and good scalability. Typical MTJ architecture consists of a paraelectric insulating tunnel layer sandwiched by two ferromagnetic (FM) layers as schematically shown in **Figure 8**a, where the thicker one with constant magnetization is called pinned layer, and the thinner one with switchable magnetization is called free layer.[231,232] An antiferromagnet is usually coupled with the pinned layer to prevent the switching of magnetization through exchange bias.

The conductivity of MTJ relies on the relative magnetization orientation between two parallel FM layers, the modulating flexibility of which constitutes the cornerstone of reconfigurability. Parallel magnetizations of the two FM layers correspond to low ohmic state (R_p) of MTJ, while highest resistive state (R_{AP}) is accessed when the configuration is antiparallel. Current-induced efforts, such as STT and SOT, can manipulate the magnetic orientation of free layer in MTJ. It's worth noting that MTJ is highly compatible with back-end-of-line process of CMOS. Combined with its geometric maneuverability that brings about numerous functions, MTJ has shown great potential for neuromorphic computing like stochastic neuron[224] and reservoir computing.[233,234]

As the mainstream of current research, STT-based MTJ[222,223,233,235,236] exhibits diverse magnetic dynamics which hold promise in reconfigurable neural networks, such as spin torque nano-oscillator (STNO),[236] spin torque transfer RAM (STT-RAM),[223,235] superparamagnetic tunnel junctions.[217] The nonlinear transient dynamics of STNO can be leveraged to implement diverse neuromorphic computing, such as spoken-digit recognition and reservoir computing.[220,234,236] Romera et al. presented that STNO can achieve temporal-pattern recognition tasks by mimicking brain-like binding events.[221] Based on the outstanding mutual-synchronization ability of STNO over wide information ranges, a high recognition accuracy of 94% was achieved by modulating the oscillator frequencies over large direct input ranges. Meanwhile, multilevel STT-RAM recently emerged as an alternative storage device for its ultralow leakage and high integration performance, which is suitable for the on-demand design of BNN accelerators.[235] By emulating intrinsic error resilience of biological intelligence, a reconfigurable STT-RAM for acceleration of various learning models has been demonstrated with precision scaling and switchable multiple modes of computing capacity, which provide an energy-efficient approach for generally proposed neural network accelerators.

5.2. Spin Orbit Torques

Beyond conventional STT-based modulation, SOT, as an extended electrically controlled spin torque on the basis of spin-orbit interaction, highlights another promising approach for reconfigurable neuromorphic electronics. For comparison, the STT-driven MTJ is controlled by a perpendicularly polarized current which always employs two-terminal configurations. While the SOT arises from transverse nonpolarized current-induced spin current, employing a three-terminal architecture for enhancing the durability of tunnel barrier and tunneling magnetoresistance ratio.[237–239] The conventional physical mechanism of SOT can be comprehended by the bulk spin Hall effect and the interfacial Rashba–Edelstein effect. Compared with STT mentioned above, SOT-based devices present several advantageous characteristics over that of STT including decoupled write/read paths,[240,241] sub-nanosecond-scale switching of perpendicular polarization,[242] and extraordinary charge-to-spin current conversion efficiency.

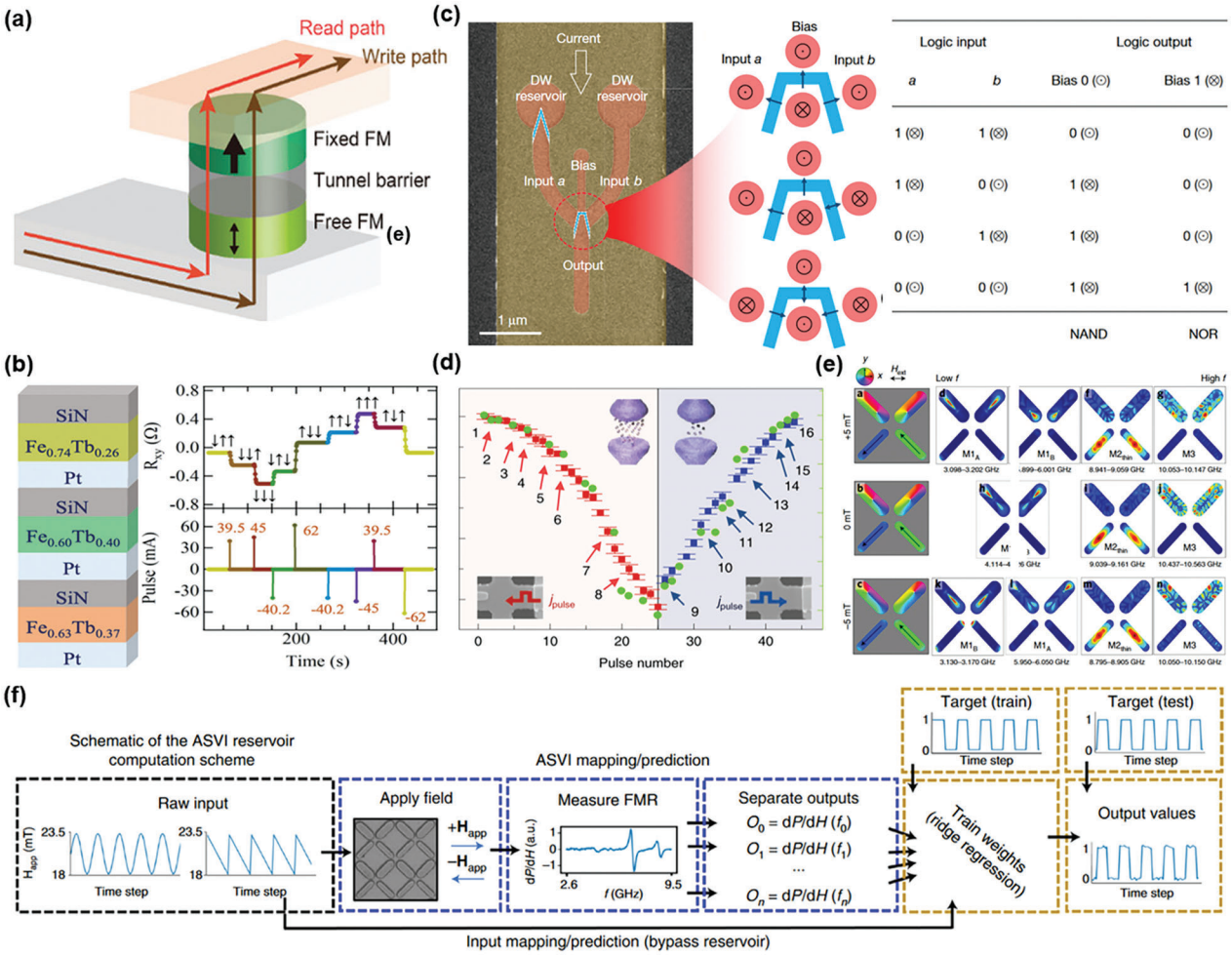

Figure 8. Spintronic mechanism-based reconfigurable neuromorphic electronics. a) Schematics of the STT-driven MTJ devices with typical two-terminal architecture. Reproduced with permission.[239] Copyright 2020, John Wiley and Sons. b) Reconfigurable magnetization configurations of multilayers for in-memory computation. Left: Schematic illustration of the triple-layer spintronic architecture. Right: Current-induced reconfigurable switching of magnetization configurations. Reproduced with permission.[244] Copyright 2020, John Wiley and Sons. c) Reconfigurable NAND/NOR logic gates driven by dynamics of domain walls. SEM image of a reconfigurable domain-wall logic gate (left); The relationship between bias, input, and output for a NAND gate (middle); The truth table for reconfigurable Boolean computation. Reproduced with permission.[64] Copyright 2020, Springer Nature. d) Skyrmion-based reconfigurable synapses. Reproduced with permission.[249] Copyright 2020, Springer Nature. e) Magnetization states of an ASVI vertex. f) ASVI-based reservoir computing scheme. Reproduced with permission.[65] Copyright 2022, Springer Nature.

The importance of SOT-induced reversible magnetization switching in developing reconfigurable in-memory logic and multilevel memory with eco-friendly and excellent computing performance has been presented recently.[243–246] Based on IrMn/Co/Ru/CoPt/CoO magnetic heterojunction device, Fan et al. modulated a single device into four independently switchable magnetic configurations at will.[246] By operating the orientation of external magnetic field and current pulse, flexible manipulation of in-plane and out-of-plane exchange bias, respectively stemming from IrMn/Co interfacial antiferromagnetic coupling and uncompensated antiferromagnetic spin reorientation of CoPt/CoO interface, was simultaneously realized. Benefiting from the reconfigurable on-demand modulation of dual exchange bias, nonvolatile 10-state memory and multiple logic functions at single-device level were then achieved, presenting the prospect of multidimensional reconfigurable neuromorphic applications such as binary convolutional neuronal networks.[117,224,239,247] Additionally, by purely electrically-controlled SOT switching, Zhao et al. modulated both exchange bias and SOT switching and implemented reprogrammable complete Boolean logic functions in a single heterojunction.[245] Dong et al. achieved reconfigurable multifunctional in-memory logic utilizing perpendicularly constructed $[Pt/Fe_{(1-x)}Tb_x/Si_3N_4]_n$ multilayers,[244] which enable electrical reconfiguration of 2^n states through SOT (Figure 8b). These 2^n memory states were further qualified to conduct scalable Boolean logic functions with high reconfigurability such as 2–2^n decoders. And the neuromorphic reconfigurability was also envisioned by this 3D spin-orbit architecture.

Reconfigurable logic-in-memory electronics mentioned above have been substantiated of great potential in promoting the energy-efficient neuromorphic computing such as BNNs. In

contradistinction to approximate computing, deep learning as a high-accuracy neuromorphic processing strategy has substantial optimized computational performance for vast data. While conventional deep learning model such as GPU-based convolutional neural network has provided a feasible scheme, it still suffers from incompatibility between operation speed and granularity owing to the data-intensive computation. Based on single-precision data communication, BNNs, have emerged as a preferable solution for Deep neural networks(DNNs), and can be improved with the reconfigurable in-memory logic using spin-orbit torque magnetic random access memory (SOT-MRAM).[223,247] Researchers have shown that the proposed SOT-MRAM can perform deep learning tasks using reconfigurable in-memory logic.[117] Benefiting from XNOR topology, this spintronic logic-in-memory XNOR neural network enables an eco-friendly binary convolution, achieving 1.2-fold energy reduction compared to the state-of-art binarized convolutional neural network hardware.[248]

Notably, although the reconfigurable logic-in-memory paradigms of SOT have been broadly implemented, other properties of SOT such as stochastic behavior for mimicking biologic probabilistic computation haven't been experimentally verified yet. Continuous efforts are actively being devoted to the field of SOT-based reconfigurable neuromorphic hardware and the emerging attempts to develop the performance of this kind of devices go into two mainstreams: ultrafast electronics facilitated by antiferromagnetic layers or ultralow-energy electronics derived from magnetic insulators. Moreover, novel mechanisms for generating spin currents, such as orbit Hall effect, will lead to deeper understanding of SOT and further improve the modulation efficiency.

5.3. Domain Walls

Domain walls, as one kind of magnetic textures, are considered to be prospective vectors of information on account of its speedy motion, high density, non-volatility, and near-zero leakage. Employing multilevel devices based on domain walls, nonvolatile memory for artificial synapses can be smoothly implemented where the broad freedom of neuromorphic parameters can be stimulated by displacement of domain walls. Moreover, the domain wall can be reversibly written, erased, and set into multiple reconfigurable electronic states which is important for general-purpose neuromorphic computing. Nevertheless, the full-blown implementation of domain walls in post-CMOS computing architecture is often limited by requirement of extra magnetic field for its manipulation and clocking, significantly impeding their large-scale integration. Here, we will introduce some state-of-art attempts in magnetic field-free domain wall-based reconfigurable device which present potential in neuromorphic computation.

The magnetic field-free scheme for reconfigurable logic-in-memory devices using full-electrical-control domain-wall racetracks was demonstrated by Luo et al.[64] Based on the out-of-plane magnetic Pt/Co/AlOx NWs with V-shaped in-plane regions, the fundamental Boolean logical values "0/1" was realized according to the polarization directions. These reversible transformations of logic are conducted by SOT-induced domain wall motion,[250–252] utilizing chiral interconnection[253] of competing magnetic anisotropy and interfacial Dzyaloshinskii–Moriya interaction,[254] which are exploited to achieve a basic inverter unit with pJ-level energy consumption. They further demonstrated a reconfigurable NAND/NOR gate (Figure 8c), the reconfigurability of which originates from the on-demand switchable orientation of electrical bias. Moreover, based on similar physical mechanism, binary full adder, and all Boolean logical functions can be implemented by directly cascading, encouraging the way for logic-in-memory neuromorphic implementations.

Beyond domain wall-based reconfigurable logics, all-electric magnetic DNNs accelerators applying intrinsic linearity of domain walls also attract many attentions. Siddiqui et al. demonstrated a purely electrically-controlled domain-wall-based neuromorphic accelerator that can implement both multilevel linear synaptic weight and programmable nonlinear neuronal activation function generation.[63] Benefiting from as-adopted three terminal MTJ architecture, current-induced SOT can manipulate domain wall dynamics in a field-free manner. This kind of programmable design allow domain-wall-based devices to be engineered into multiple reconfigurable roles within a neuromorphic accelerator, such as synaptic weight generators and neuronal behavior simulators. The proposed domain-wall technology achieves nanosecond-level operation and pJ-level consumption, which present bio-comparable power efficiency and versatility advantages over other hardware implementations for realizing deep neural networks.

5.4. Skyrmions

Skyrmions, one of the topologically protected magnetic textures that stabilized by the Dzyaloshinskii–Moriya interaction, were first proposed for describing hadron and observed in magnetic material.[248,255,256] Benefitting from their nanoscale dimension, non-stochastic characteristics derived from topological-screening depinning, and relatively low threshold current compared with domain walls, skyrmions show huge potential in high-integration and low-power neuromorphic electronic paradigms.

Previous works show that the conversion stimulated by motion and annihilation of skyrmions have been utilized to realize reconfigurable Boolean logic gates,[257] neuronal LIF characteristics,[258,259] synaptic multiple plasticity,[249,260] and other biorealistic functions. Particularly, biologic neurotransmitter dynamics can be emulated by engineering skyrmions, owning to their particle-like behavior and thermal Brownian motion.[218] Additionally, Luo et al. designed a reconfigurable skyrmion logic device with complete Boolean logic functions.[257] Benefiting from pure-skyrmion mechanism, the motion and interaction of skyrmions can be simply manipulated utilizing terminal voltage to implement device-level reconfigurable logics (e.g., AND, OR, NOT, NAND, NOR, XOR, and XNOR), driven by spin-orbit torque, skyrmion Hall effect, skyrmion-edge repulsions, and the voltage control of magnetic anisotropy effect.

In the context of neuromorphic computing, nonlinear resistive effect of skyrmion devices, deriving from incorporation of tunneling non-collinear magnetoresistance,[261,262] anisotropic magnetoresistance and spin-torque effects,[263] allows for processing unconventional computing event such as reservoir computing.[264,265] Meanwhile, the demonstration of reconfiguring the input data streams has been smoothly implemented

by thermal diffusive dynamics of skyrmions.[218,228] Zázvorka et al. employed pure skyrmion diffusion in multilayer system to achieve a skyrmion reshuffler, which could be controlled by both out-of-plane field and current injection. Such a skyrmion reshuffler is the core building block for the novel energy-efficient stochastic computing and possesses extraordinary fidelity which can be subsequently qualified as LIF neurons.[218] Furthermore, Song et al. demonstrated all-electric skyrmion-based synaptic devices at room temperature, which utilize the current-controlled SOTs to induce generation and annihilation of skyrmions.[249] The dynamics of skyrmions could imitate 16 reconfigurable synaptic state parameters by controlling the number of skyrmions (Figure 8d). This skyrmion-based synapses can further imitate neural networks using array architecture, which achieve distinguished pattern recognition with an accuracy of ≈89%.

The development of skyrmion-type devices for neuromorphic applications is still in infancy, where the inevitable disadvantages such as large unit-cell area and relatively low on/off ratio significantly hinder their prosperity. However, the distinct particle-like and topographic-defect immunity of skyrmion-type spintronics highlights their superiorities over conventional RRAM-based schemes, presenting their enormous potential in reconfigurable neuromorphic applications.

5.5. Artificial Spin Ice

Artificial spin ice (ASI) is a sort of metamaterials that employs nanomagnets for representing manufactured macrospins where geometrical frustration can be artificially accommodated.[266] Typical ASI system sustains two main magnetic textures including Ising-like macrospins in nanoislands and vortex states in nanodiscs. By tailoring magnetic elements through nanofabrication, complex "designer" effects are observed, endowing the ASI systems large freedom space, which subsequently enable multiplicity of programmable configurations through external applied magnetic field. Reconfigurable, non-volatile artificial magnetic ice, which is now often referred to as ASI, was introduced as early as 2006 by Wang et al. to study the accommodation of geometrical frustration in a square lattice of elongated interacting ferromagnetic nanoislands.[267] Since then, various experimental phenomenon such as spontaneous long-range ordering,[268,269] emergent "magnetic monopole" defects,[270,271] and the tailorable material-by-design properties,[11,272] have been explored for the employments of ASI devices, showing great material-level reconfigurable potential in neuromorphic computing.

Beyond the aforementioned advantages of ASI, one of the difficulties is how to realize long-range ordered orientation of ASI configurations which might provide novel perspectives on spintronic research. This issue was solved by Wang et al. in 2016 by using three-rotational-symmetry ferromagnetic nanoislands to replace conventional fourfold symmetry square lattices.[229] Gartside et al. in 2018 provided approaches to the nearly all-around potential microstates of ASI induced by geometrical frustration, from ground state to high-energy "monopole-chain" state.[268] By taking advantage of reconfigurability in ASI system, they further achieved microstate-dependent mode-hybridization and anticrossings which invite a host of Boolean logic and neuromorphic applications.[223]

Reconfigurable ASI structure can also be combined with superconductors,[273] exhibiting distinct high degeneracy and subsequently diverse microstates, which could illuminate an approach to modulate reconfigurable neuromorphic state parameters by controlling ASI magnetic configurations.[274] Wang et al. successfully derived multiplicity of eight configurations of magnetic charges by utilizing 2D magnetic field-assisted magnetic force microscopy patterning technology.[229] They further demonstrated globally reconfigurable write-read-erase multifunctionality by simply programming in-plane vector magnets at room temperature. This rewritable ASI provides a precise-control template of unit-cell-level state parameters, which shows the potential for neuromorphic synaptic devices. Beyond the conventional ASI platforms which comprise a single magnetic texture, another emerging idea is to engineer the macrospin-vortex bistability for richer reconfiguration of neuromorphic electronics. Gartside et al. demonstrated a brain-inspired hardware platform with "artificial spin-vortex ice" (ASVI),[65,67] which promise to construct a lower-energy reservoir-computing system using spin-wave microstate fingerprinting (Figure 8e). The ASVI is a nanomagnetic array with strong interaction presented by tailoring nanocomponents, typically comprising two Ising-like macrospin orientations and two vortex chirality. Benefiting from this fourfold bi-textured property and non-volatile magnetic states, ASVI offers physic memory phenomena and magnonic reconfigurability reflected by huge frequency shift (far surpasses the GHz shifts available in conventional all-macrospin ASI). The researchers further employed the ASVI to implement a magnonic reservoir computer, an unconventional genre of neural network which particularly appropriate to dynamical situations (Figure 8f). The ASVI-based computer could realize chaotic time-series forecasting and study linear and non-linear signal transformations with ultralow mean squared error, which is competitive with existing reservoir computing schemes. This extraordinary performance of ASVI as neuromorphic building blocks was attributed to indefinite non-volatile data storage, electrical connection-free scheme, and high reconfigurability.

6. Photonics

Significant progresses have been made in neuromorphic computing in the field of electronics, from exploring potential promising electronic information materials, which have been used to emulate flexible, robust, and vivid basic components of ANNs (e.g., synapses and neurons),[10] to building energy-efficient neuromorphic architecture based on conventional CMOS.[13,14,89] Although these emerging electronic elements and frameworks have provided an effective way for emulating animate neural networks to speed up the processing of tasks in mathematical processing,[47,275] image classification,[167,276] speech recognition,[277] etc., parallelly solving multiple complex problems efficiently as the biological brain on distributed electronics with dense hardwire interconnections is still an enormous challenge due to latency and bandwidth constraints.[278] Photonics based on optical interconnections and linearity are promising approaches to alleviate this problem and provide another angle of view to accelerate neuromorphic computing.

Inherent boson property which enables lights of several wavelengths or modes to transmit through the same photonic data

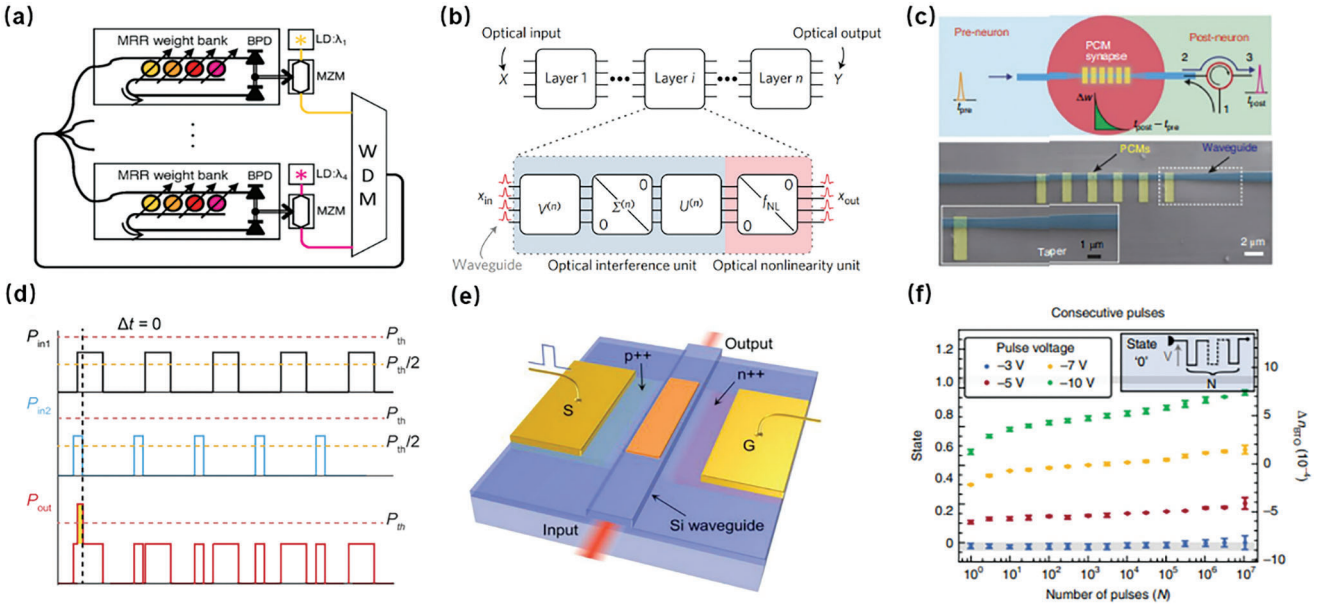

Figure 9. Neuromorphic photonic synapses. a) Broadcast-and-weight protocol using MRRs as tunable filters to weight WDM signals. Reproduced under terms of the CC-BY license.[286] Copyright 2017, The Authors, published by Springer Nature. b) OIU that compose each layer of the neural network to implement real-valued matrix. Reproduced with permission.[288] Copyright 2017, Springer Nature. c) Photonic synapse implemented with discrete PCM islands. d) Pre- and postsynaptic signals with no time delay under STDP rule. Reproduced with permission.[289] Copyright 2017, The American Association for the Advancement of Science. e) Schematic of the non-volatile reconfigurable photonic switching unit. Reproduced with permission.[290] Copyright 2022, IEEE. f) Modulation of ferroelectric domain states using consecutive pulses with different voltage amplitude. Reproduced under terms of the CC-BY license.[291] Copyright 2021, The Authors, published by IEEE.

link at ultrahigh speed makes photonics uniquely advantageous in bandwidth, latency, and propagation efficiency, averting many trade-offs in neuromorphic electronic approaches.[22,278] Moreover, silicon-integrated photonics can host active and passive optical (or optoelectrical) components simultaneously enabling competitive integration density,[279,280] and allowing implementations for linear operations in the optical domain.[281] So far, many neuromorphic computing techniques have been demonstrated based on integrated photonics and free-space optics to realize neural isomorphism (usually mathematically isomorphic to neural network algorithm), ranging from critical elements in different kinds of neural networks to specialized hardware accelerators in AI solutions.[92,282,283] Although photonics possess exclusive advantages over electronics in parallelism and linear operations, new challenges such as thermal stability, all-optical nonlinear elements, and light sources on-chip call for in-deep investigations.[22] Thus, neuromorphic photonics should not be expected to develop separately, instead, continuous research is required to combine the advantages of photonics and electronics, toward an ultimate neuromorphic photonic architecture.

In this section, we introduce photonics for matrix multiplication, nonlinearities, and neuromorphic architectures, corresponding to biological synapses, neurons, and neural networks, and focus on the reconfigurability of these implementations.

6.1. Photonic Synapses

Neuronal dense connections weighted by synapses are the key for rich dynamics in biological brain. To mimic various behaviors of the brain, reconstruction from physical primitives for connected units and strengths has been proven to be an effective method. The connected strengths can be represented by a weight matrix that can multiply input signals of neurons; While the connected units, namely neurons, require not only nonlinear responses but also fan-in and cascading property.[22]

One kind of optical implementation for synapses is based on wavelength. Optical signals are weighted by tunable waveguide components and can be accumulated through wavelength-division multiplexing (WDM), which is widely employed in the demonstrations of multiwavelength synapses. By using WDM, a protocol called broadcast-and-weight was proposed to control connections and weights.[284] It consists of a group of nodes sharing a common waveguide where a unique transmission wavelength is assigned to each node. With reconfiguring a spectral filter bank at each node's front-end, various network patterns could be determined. Based on this protocol, microring resonators (MRRs) were used as tunable filters to weight WDM signals, and a recurrent silicon photonic neural network was demonstrated successfully (**Figure 9**a).[285,286] Another way to weight connections is based on optical modes. A real-valued matrix may be represented as $M = U\Sigma V\dagger$ through singular value decomposition, in which U, $V\dagger$ can be implemented with an array of beamsplitters and phase shifters,[287] while rectangular diagonal matrix Σ can be implemented using optical attenuators.[281] To implement any weight matrix M, optical interference unit (OIU) was proposed and demonstrated experimentally in a silicon photonic integrated circuit using a mesh of 56 reconfigurable Mach–Zehnder interferometers (MZIs), as shown in Figure 9b, each of which has a phase shifter between two directional couplers,

followed by another phase shifter.[288] By setting internal and external phase shifters, the MZI splitting ratio and differential output phase were controlled and the programmable nanophotonic processor which consisted of four layers of OIUs (with four optical neurons to add nonlinearities) was implemented, achieving recognition accuracy of 76.7% on the vowel identification test set.

In addition, hardware synapse implementations that modulate effective refractive index of waveguides by optical or electrical actuation approaches have been demonstrated. Cheng et al. reported an all-optical synapse using tapered waveguide structure and discrete chalcogenide PCM islands (Figure 9c),[289] enabling effective control of non-volatile synaptic weights by changing the number of optical pulses, and the STDP rule in biological system was mimicked by arranging the pre- and post-synaptic signals (Figure 9d). To obtain scalable integrated and energy-efficient switching units in a CMOS-compatible process, non-volatile reconfigurable photonic switches actuated by silicon PIN diode heaters were demonstrated by Zheng et al,[290] as shown in Figure 9e. They integrated chalcogenide $Ge_2Sb_2Te_5$ on PIN diode heaters, where the electrical pulse-generated Joule heat can trigger phase transitions and thus control the refractive index of waveguides. Subsequently, electrically modulated switching units on microring resonators were fabricated, with high endurance (> 500 cycles) and near-zero additional insertions loss (≈0.02 dB μm^{-1}). Although PCMs are commonly used for non-volatile photonic applications due to long endurance, small footprint, and high scalability, they face challenges in controlling the phase transitions and asymmetry in the energy when transforming between amorphous and crystalline states,[291] limiting the repeatability of potential reconfigurable functions. Recently, an alternative solution was presented by Geler-Kremer et al.[291] By using ferroelectric $BaTiO_3$ thin films embedded in compact waveguides, the switching of ferroelectric domain corresponds to the change of electro-optic response. Therefore, a brand-new non-volatile modulation method depending on the pulse width, amplitude, and repetition of control signals was provided (Figure 9f). Compared with traditional non-volatile photonic elements which mostly focus on PCM, the $BaTiO_3$-based phase shifter demonstrated salient metrics performance, realizing eight repeatable, distinguishable, and equally spaced states. For next-generation programmable photonic platforms, kinds of non-volatile, reconfigurable phase shifters will be well applied and likely to promote the development of the field.

6.2. Photonic Neurons

Pure linear operations are not enough to process information efficiently. Thus, emerging photonic approaches to realize neurons' nonlinearities have been proposed. Huang et al. demonstrated a reconfigurable photonic-electronic neural network which integrates photonic neurons on chip and can be programmed to perform various tasks.[292] As shown in **Figure 10**a, the input signals are weighted in parallel with MRRs and then summed by a balanced photodetector implementing positive and negative weights, generating a photocurrent to modulate the transmission of the ring modulator serving electro-optic nonlinearity. It involves the nonlinear conversion of optical- into electrical- and back into optical signals in this process. All-optical neurons do not expect the transmission signal in the form of photocurrent, but instead, represent it as the changes in material properties. A neuronal ring resonator with independent integrated PCM cells was implemented to generate spike signals (Figure 10b),[293] in which the neuronal PCM cell can be switched between the crystalline and amorphous states depending on the incoming weighted power of pre-synaptic neurons, changing the optical resonance condition of the ring and propagation loss to emulate the basic integrate-and-fire function of the neuron.

In addition to artificial neurons relying on integrated photonic devices, ones based on free-space photonics have been implemented into the all-optical neural network. For example, Zuo et al. achieved different nonlinear activation functions for various neurons by placing the coupling-probe beams at different positions of the magneto-optical trap, while the linear operations were implemented by spatial light modulator (SLM).[294] The optical neural networks in free-space will be described in detail in the next part. While specialized photonic neurons have been widely reported, we believe general-purpose photonic integrated signal processors (PISPs) may also be used to perform reconfigurable signal processing functions, which are potentially applied to process neuronal signals. Liu et al. proposed a fully reconfigurable PISP based on an InP-InGaAsP material system.[295] By incorporating nine semiconductor optical amplifiers and twelve current-injection phase modulators in the unit which consists of three active MRRs and a bypass waveguide, three signal processing functions including temporal integration, temporal differentiation, and Hilbert transformation were obtained.

6.3. Photonic Neural Networks

Most implementations of photonic neural networks fall into two broad categories based on integrated photonics and free-space optics, respectively. The main differences between these efforts are attributed to the concrete method to emulate synapses and neurons as well as network topology. As we discussed above, various optical hardware configurations can be implemented to realize weighted connections (synapses) and nonlinear activations (neurons), and thus developing one or more general protocols for assembling these basic elements may unlock more powerful and reconfigurable networks. And the network topology, which describes the interconnections between neurons, mainly centers on feed-forward and recurrent structures in most of the current demos.

Figure 10c shows one feed-forward and spiking architecture of a single layer from an optical neural network integrating a WDM multiplexer, PCM synapses, and ring resonator neurons.[293] In this scalable architecture, supervised and unsupervised learning is enabled and pattern recognition can be demonstrated directly in the optical domain. Figure 10d shows the matrix multiplication unit based on MZIs, and nonlinear activation function is considered to associate with a realistic saturable absorber.[288] This architecture also enables new methods to train an optical network without back propagation and gradient descent. By using forward propagation and the finite difference method, the gradient of each parameter could be obtained and a vowel recognition problem was solved. Furthermore, combining semiconducting few-photon light-emitting diodes with superconducting-nanowire

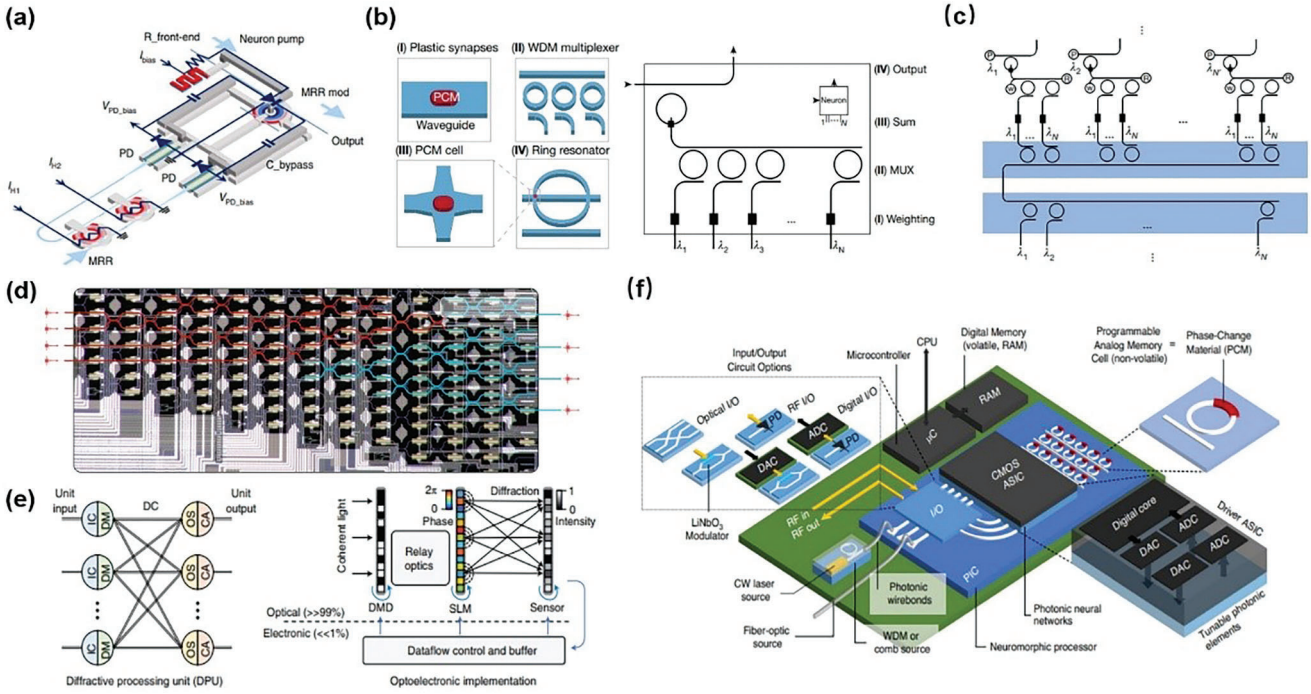

Figure 10. Neuromorphic photonic neurons and networks. a) Photonic neuron implemented with balanced photodetector (BPD) and MRR mod. BPD generates weighted photocurrent with a bias current and modulate the transmission of the MRR modulator via free-carrier injection. Reproduced with permission.[292] Copyright 2021, Springer Nature. b) The all-optical spiking neuron using PCM cells. Reproduced with permission.[293] Copyright 2019, Springer Nature. c) A single layer of all-optical neural network integrating a WDM multiplexer, PCM synapses, and ring resonator neurons. Reproduced with permission. Reproduced with permission.[293] Copyright 2019, Springer Nature. d) Experimentally demonstrations of coherent nanophotonic neural network enabling both matrix multiplication and attenuation. Reproduced with permission.[288] Copyright 2017, Springer Nature. e) Left, the diagram of diffractive processing unit (DPU) as a computing building block. Right, a DPU implementation using reconfigurable optoelectronic devices. f) A conceptual neuromorphic photonic processor architecture employing both electronic and emerging photonic technology. Reproduced with permission.[292] Copyright 2021, Springer Nature.

single-photon detectors to behave as spiking neurons which connect via optical waveguides, superconducting optoelectronic devices with tunable weights of connection were implemented.[76] The weight updating mechanism is demonstrated with the employment of electromechanically actuated waveguide couplers, in which the distance, as a function of the synaptic weight matrix, can be modulated by the externally applied voltage which gives rise to an attractive force. Benefiting from the proposed reconfigurable neuromorphic elements, a multilayer perceptron and an artificial visual system with temporal processing and interference suppression were proposed.

In addition to integrating photonic devices on chip, free-space diffractive network is another kind of implementation for neuromorphic photonics. Zhou et al. proposed the reconfigurable diffractive processing unit (DPU) based on diffraction light, which could be programmed to change its functionality and build different types of ANNs including diffractive deep neural network, diffractive network in network, and diffractive recurrent neural network.[296] In DPU, as illustrated in Figure 10e, a digital micromirror device and a SLM (as an important component to achieve reconfigurability), are used to quantize and convert unit input data to a complex-valued optical field to implement the input nodes, which are connected to output neurons with the light diffractive connections determined by the modulation of the wavefront. And a CMOS sensor is selected to sum weighted signals and implement activation function during the photoelectronic conversion. Moreover, an active reflective graphene-plasmonics-based SLM was employed in the terahertz DONN with validation accuracy >94% on the MNIST dataset.[297] The above examples show exciting and promising applications of machine learning due to reconfigurable key elements and scalable photonic platforms, while the critical challenges are co-designing of electronics and photonics on an unified processor architecture. A conceptual photonic processor was described (Figure 10f),[292] which needs a perfect silicon photonic platform converging both mature and emerging technologies such as monolithic fabrication, tunable photonic elements, and photonic neural networks. Depending on modern integrated platforms for reconfigurable photonics, neuromorphic photonics exhibits great potential to accelerate information processing.

7. Integrated Reconfigurable Neuromorphic Computing

Brain-inspired computing, introduced for apperceptive and cognitive assignments, contains two mainstreams: computer-science-oriented ANNs and neuroscience-oriented spiking neural networks (SNNs),[12] which have made substantial progresses in dealing with intricate large data.[92] Computer-science-based ANNs, as the mature approach, partly assimilate the

characteristics of cortex in light of spatial complexity, exhibiting fairly high potential in image recognition, language classification, and so on. In contrast, SNNs, as a more biomimetic approach, adopt temporally sparse spikes training as well as event-driven and localized information processing strategies in a massively parallel manner, exhibiting great potential for releasing reluctant resource occupation by minimizing data transformation, which aims at fully exploring the efficient capacity of neuromorphic computing.[4,9,79] While neuromorphic systems have shown well-known eco-friendly advantages, it remains difficult to be compatible with mature preparation technology. Here, we will introduce a set of strategies, including CMOS-based and resistive random-access memory (ReRAM)-based neuromorphic systems, which provide opportunities in promoting the development of integrated reconfigurable neuromorphic computation.

7.1. Neuromorphic integration Implemented with CMOS-Based Devices

With the prosperity of the mature silicon technology, CMOS-based neuromorphic integrated system is one of the headmost neuromorphic computing paradigms, which can take full advantage of cutting-edge silicon technology and show great compatibility with other artificial intelligence technologies.

As one of the most extensively adopted reconfigurable architectures, field programmable gate array (FPGA) with matrix of configurable logic blocks and complex interconnection routing to be customed on demand, has been broadly used as accelerator board for neuromorphic hardware owing to the flexibility of semi-customized characteristics.[88,97,298–300] Reconfigurability of FPGA mostly stems from reprogrammable routing architecture which consumes ≈ 90% of the FPGA resources. Meanwhile, look-up tables, the key functional component of configurable logic blocks, can be fully assembled to realize programmable logic functions, which also contribute to FPGA's reconfigurability. Inspired by the human brain's biologically-efficient parallel capability, SpiNNaker, one of the FPGA-based SNN architectures, has been proposed for real-time simulation of neuronal hardware.[88] The multiprocessor adopted globally asynchronous interconnection infrastructure for power efficiency and encapsulated locally synchronous sections in between for decreasing time delay, which marginally reduced the trade-off between time and energy efficiency. Benefiting from the extraordinary reconfigurability of SpiNNaker's multiprocessor which contains 18 ARM968 processors to be dynamically customized, this scheme is capable of emulating biomimetic connectivity to sufficiently configurate billions of spiking neurons and achieving high flexibility in the case of invoking FPGA. Optimized algorithm-promoted SNN also extends a promising step toward system-level emulation of SNN. Wu et al. proposed a reconfigurable SNN scheme employing fast-convergence coordinate rotation digital computer (CORDIC) algorithm for faster real-time STDP learning and higher energy efficiency.[97] Utilizing time-division multiplexing strategy assisted with FPGA, dynamical reallocation of the neuronal spiking data into corresponding synaptic arrays was implemented, which is conducive to enhancing hardware efficiency (**Figure 11**a). This programmable SNN outperformed state-of-the-art CORDIC schemes by 38.5–45.3% in light of online learning speed and power efficiency.

Apart from mature FPGA-inspired neuromorphic platforms that mimic biological neural networks from the functional perspective,[298–300] another important thread is to structurally approximate the biological functional components from the fundamental device perspective which highlights a more biomimetic approach.[13,89] Individual neuron with various behavior functions can be independently reconfigured with a time-multiplexed circuit and each synaptic weight can be flexibly modulated, which make for successful implementation of device-level reconfigurability. At the system level, reconfigurability derives from arbitrary intra-layer neuron-to-axon intercalation by utilizing the point-to-point (P2P) routing topological strategy (Figure 11b). At the applicability level, benefiting from event-driven property and seamless scalability, researchers can successfully manage TrueNorth chip to execute multi-object detection and classification and the power is down to 26 pJ per synaptic event. Although TrueNorth chip design is capable of real-time multi-task processing, online learning ability is desperately required to expand on-demand neuromorphic applications. A few implementations about the reconfigurable on-line learning SNN processor have been demonstrated, such as ROLLS processor comprising 256 neurons and 128K synapses,[95] but the limited integration of on-line learning chip significantly hinder further improvements. Compared with TrueNorth chip, Inter's Loihi chip features an outstanding online-learning ability based on manycore mesh architecture,[89] which possesses a microcode-driven programmable learning engine that allows Loihi to perform real-time SNN training and to obtain a broadest possible class of SNN learning rules. At the specific implementation standpoint, Loihi pioneered to integrate the features of programmable synaptic spike time constants, multiple spike trace, triple synaptic state variables, and spike rewarding, all of which contribute to the reconfigurability of Loihi's SNN learning rules. Additionally, brain-inspired elements (i.e., synapses, axon) and computation (i.e., refractory delays, dendritic tree processing) were further qualified to be adaptably configured, in combination with chip's online learning abilities, which support diverse application scenarios including autonomous driving, prosthesis control, and the Internet-of-Things.

Beyond abovementioned implementations for reconfigurable neuromorphic computing, reconfigurable heterogeneous computing integrates originally incompatible computing paradigms with different coding schemes, functions, or computing architectures into a synergistic parallel-computing hardware platform. Cooperating with brain-inspired computing, reconfigurable heterogeneous computing highlights a state-of-art optimising solution for hashrate bottleneck and generalized neuromorphic hardware.[14,36,85,86,90,301–304] To actualize the neuromorphic reconfigurable heterogeneous computation, cross-modality ANN/SNN designs[14,36,90] and heterogeneous integration technology[85,86,301] as the two mainstreams from distinct aspects have shown the significant prospects which will be introduced in Subsection 7.2.

Achieving reconfigurable coordination of both ANNs and SNNs in a unified platform is an emerging heterogeneous fusion technology to solve complex dynamic problems with imperfect or uncertain data, enabling concurrent execution of diverse real-world tasks. With the substantial synergy of

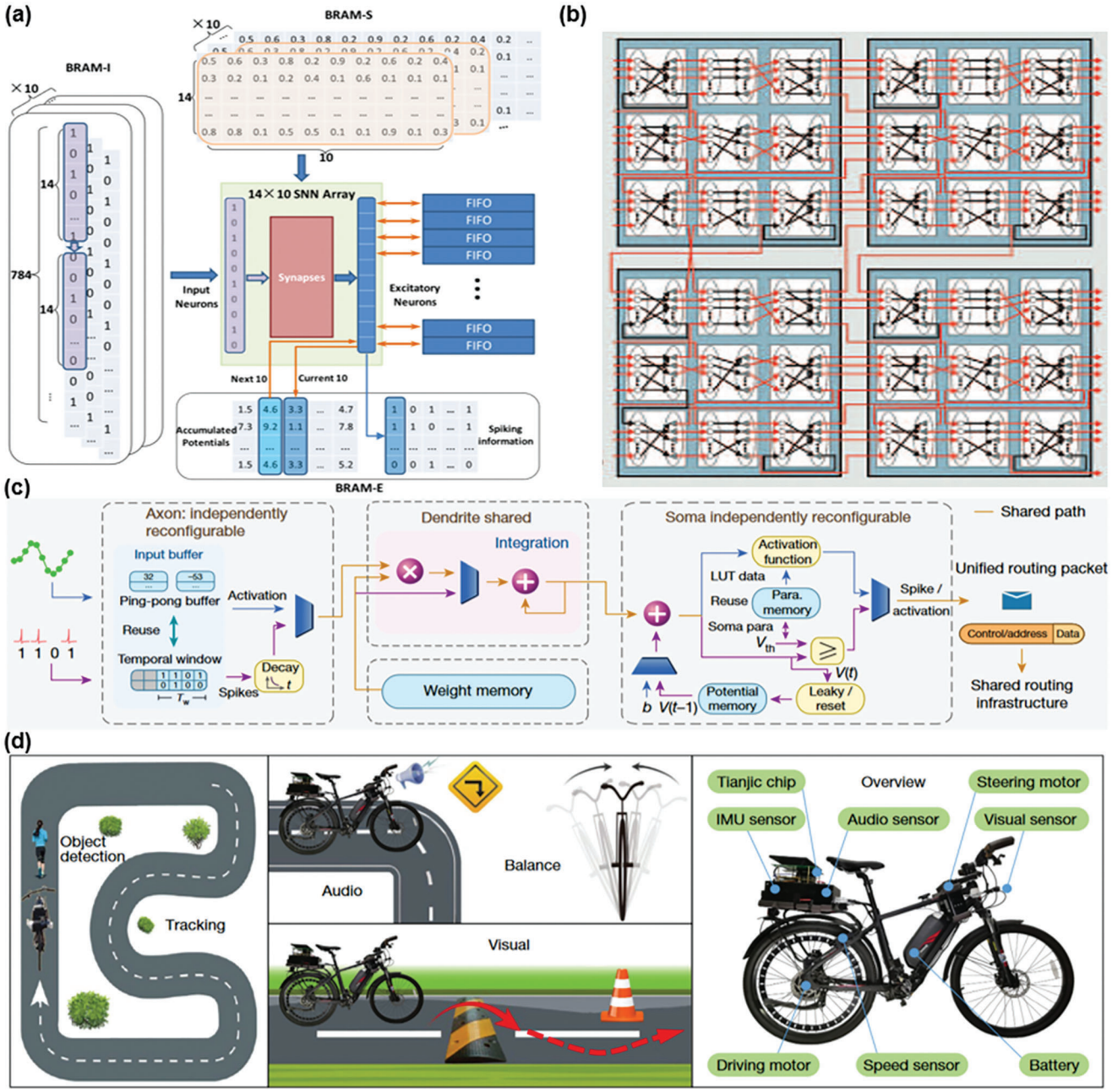

Figure 11. Reconfigurable neuromorphic computing at the integration level. a) Data flow of CORDIC-based reconfigurable SNN accelerator with TDM strategy. Reproduced with permission.[97] Copyright 2021, IEEE. b) The TrueNorth multichip architecture with reconfigurable point-to-point schemes. Reproduced with permission.[13] Copyright 2014, The American Association for the Advancement of Science. c,d) Tianji chip: c) the diagram of cross-paradigm neuron system with hybrid ANN and SNN segments, d) illustration of unmanned bicycle application. Reproduced with permission.[14] Copyright 2019, Springer Nature.

reconfigurability from device and chip level, Pei et al. have demonstrated Tianjic chip, a cross-model neuromorphic scheme with hybrid ANNs/SNNs, featuring a many-core architecture, reconfigurable building blocks and a streamlined dataflow.[14] At the device level, spike representation of binary sequences was selected to realize a compatible coding paradigm between ANNs and SNNs. This versatile system employed unified functional cores (FCore) for deep imitation of biological components, where axon, soma, and routing look-up tables can be reallocated into multiple modalities to support on-demand connection (Figure 11c). This device-level reconfigurability enables the FCore to consequently execute reconfigurability by means of flexibly assembling diverse functional primitives (axon, soma, routing look-up table, and so on). Furthermore, the Tianjic chip, supporting both ANN-based precise computing and SNN-based neuromorphic approximation, has been demonstrated to implement

driverless bicycle task with real-time object tracking, speech and balance control, as well as obstacle avoidance by operating the CNN, CANN, SNN, and MLP networks concurrently in a seamless communication manner (Figure 11d). More recently, Kuang et al. created a larger-scale hybrid-modal chip presenting reconfigurable 64 million synapses and 64,000 neurons with outstanding capacity, throughput, and efficiency.[90] Based on the LIF neuron model, this scheme featured an advanced multiplierless digital neuron system aiming at the area- and energy-efficient integration of both biomimetic SNNs and event-triggered ANNs. Reconfigurability of this scheme mainly derives from the point-to-point routing protocol and pipeline structure with the view of realizing various network topologies. Benefiting from the ultra-compatibility of point-to-point schemes for both inter- and intra-chip communication, the reprogrammable interconnection between arbitrary neurons and adaptive control of single neuromorphic elements was guaranteed, which contributes to reconfigurable neuromorphic computing. Compared to above-mentioned chip, this scheme actualized highly integrated neuromorphic chip, while its limited event-based properties of ANNs and shortage of sufficient practical application proofs expect further investigations on cross-paradigm reconfigurable neuromorphic chips.

7.2. Neuromorphic Integration Implemented with ReRAM-Based Devices

In addition to the abovementioned CMOS-based designs of neuromorphic computing systems, the development of neuromorphic electronics such as ReRAM provide a promising insight into resolution of memory wall challenge and implementations of area- and energy-efficient bioinspired computing platforms. Although many recent investigations have shown fully integrated ReRAM neuromorphic chips are capable of reprogrammable multiply-accumulated operations for AI edge computation and other neuromorphic applications,[305–308] it remains challengeable to simultaneously deliver efficiency and versatility to achieve various neural networks and software-comparable accuracy. And the existing ReRAM schemes still suffer from stochasticity, poor endurance, limited intra-block communication and hardware overhead (e.g., peripheral control circuitry and analogue-to-digital converters), impeding the sufficient utilization of ReRAM's high efficiency and density.[99,309,310]

Pioneering works on building neuromorphic hardware platform with ReRAM to solve abovementioned issues have been achieved. In 2019, a full-chip stack solution of ReRAM-based process-in-memory neural network accelerator—a reconfigurable architecture has been created by Ji et al.,[15] which contains field programmable synapse array (FPSA) and the corresponding software hierarchy where this hierarchy reconfigures the hardware resource provided by FPSA. FPSA contains spiking memory blocks and configurable logic blocks which are interconnected through a reconfigurable routing architecture, contributing to overcome exiting communication bottleneck. Contrary to abovementioned SpiNNaker based on ASICs, FPSA is a non-ASIC scheme and first adopts the ReRAM-based reconfigurable routing architecture for analog circuits, which augments the achievable computing, buffering, controlling, and wiring resources for software. FPSA' performance was qualified to outperform the state-of-art cutting-edge NN accelerators by up to 1000× speedup.

NeuRRAM—a ReRAM-relied compute-in-memory chip with a hardware-algorithm co-optimization technology, has been presented by Wan et al.,[33] which integrates power efficiency, flexibility of various neuromorphic architectures and software-comparable inference accuracy into one RRAM chip. The analogue programmability of 3 million RRAMs offers the on-demand processing granularity at the device level and tuneable computation bit-precision at the system level. From the chip-architecture standpoint, a transposable neurosynaptic array achieves reconfigurable dataflow dynamics which is feasible for implementing maximized model architectures with changeable dataflow directions in a cost-efficient and non-trade-off manner (**Figure 12**a,b). Notably, this NeuRRAM chip composes of 48 compute-in-memory cores those support reprogrammable weight-mapping strategies and a wide range of I/O dynamics at the system level. Compared with the state-of-art RRAM chips, NeuRRAM exhibits doubled energy efficiency and possesses excellent accuracy which is comparable to software simulations.

Beyond cross-paradigm combination of different neural networks introduced in Subsection 7.1, another important approach for reconfigurable heterogeneous neuromorphic computing is 3D heterogeneous integration technology which features high-density interactive interfaces with preferable bandwidth and ultralow latency, while conventional heterogeneous integration is burdened with fixed hardwire connection calling for further improvements. Based on extraordinary inter-chip stackability of 3D heterogeneous integration technology, Choi et al. demonstrated a non-von Neumann reconfigurable chips consisting of optoelectronic device arrays and memristive crossbars.[85] The former embedded in freestanding chips is made up of optoelectronic photodiodes and light-emitting diodes (Figure 12c), executing inter-chip optic communication without hardwire bonding and printing, which endows the hardware with a huge space of freedom for reconfigurability. The memristor crossbars are implanted as neuromorphic functional cores (Figure 12d) in each chip layer, implementing intra-chip parallel data processing, which contributes to enhancing processing duration and data bandwidth. To qualify the faithful reconfigurability, hetero-integrated modules consisting of optical sensor layers and multimodal processors were managed, and a corrupted letter recognition task was executed by intercalating a denoising chip into a stackable hetero-chip architecture. Benefiting from hardwire-free light interconnection, cross-modality data processing is achievable by reconfiguring and customizing functional layers on-demand, and efficient parallel computing of diverse processors by flexibly staking has also been successfully demonstrated. Notably, while the intra-layer reconfigurability remains absent in this work, the multi-granularity computation could be achieved by this modular scheme though elaborately reconfiguring the stacking orders.

8. Outlook

Reconfigurable neuromorphic computing is one of the mainstream trends for artificial intelligence to realize the general-purposed multifunctional hardware. It integrates multiple primitives into simple devices, which only require simple modulations to execute cross-modality switching for ever-changing

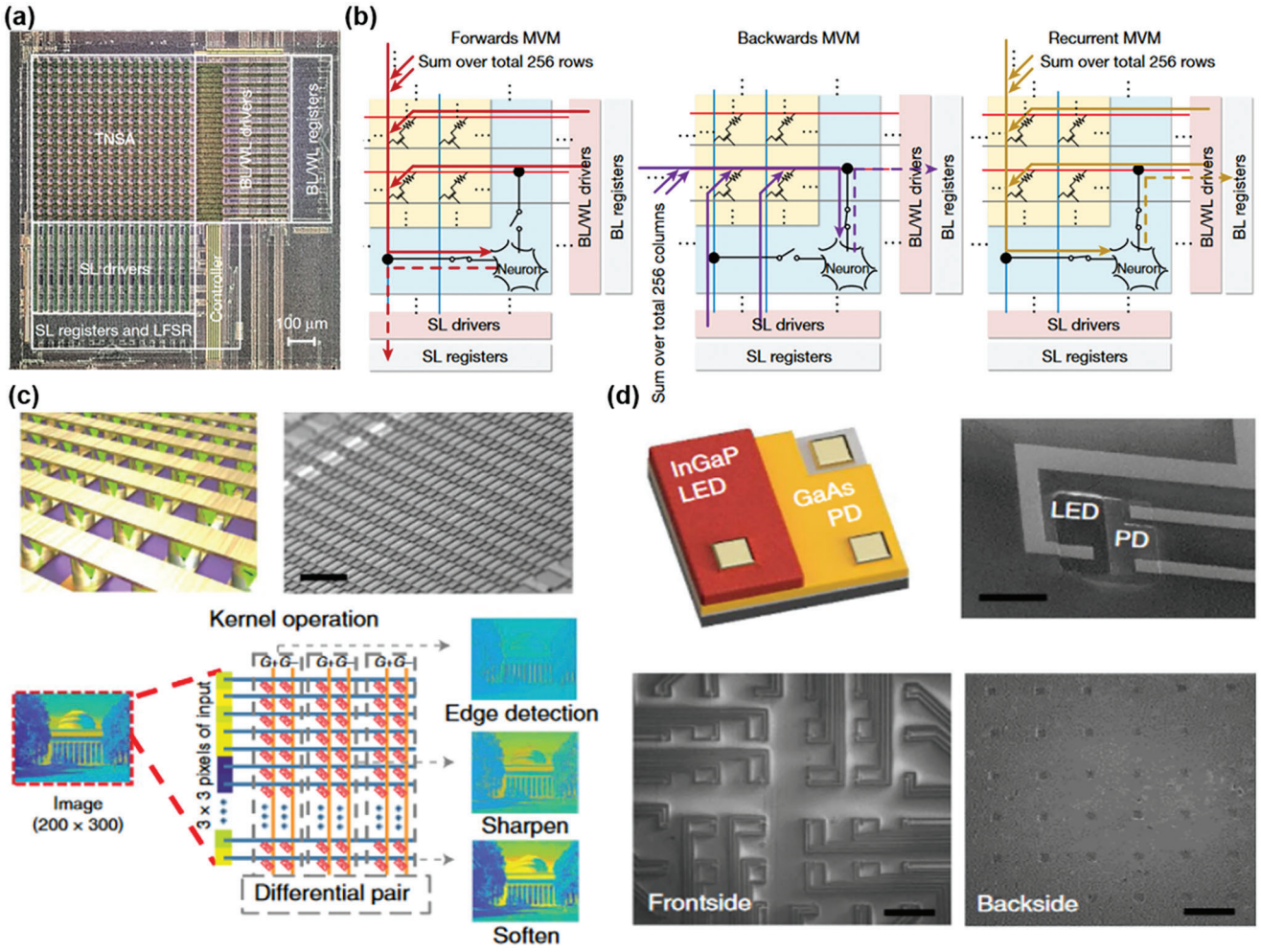

Figure 12. Reconfigurable neuromorphic computing at the integration level. a,b) Reconfigurable structure of NeuRRAM chip: micrograph of one computing-in-memory core on NeuRRAM chip (a), reconfigurable data-flow direction where the transposable neurosynaptic array can be reversibly configured in recurrent, forward or backward directions (b). Reproduced under terms of the CC-BY license.[33] Copyright 2022, The Authors, published by Springer Nature. c,d) Optoelectronic device stack (c) and neuromorphic computing core (d) of reconfigurable hetero-integrated chips. Reproduced with permission.[85] Copyright 2022, Springer Nature.

circumstances. Redundant hardware consumptions are substantially reduced, thereby relieving the pressure on hardwire connection and data transfer. Therefore, reconfigurable neuromorphic computing facilitates high versatility, integration, energy efficiency, as well as unprecedented resource reuse.

Reconfigurable capability can be comprehended from three aspects. First, reconfigurable device features manoeuvrability which can be dynamically customized to cater for different appointments. These kinds of devices aim to manage various reliable computing primitives to enhance the degree of integration and miniaturization in an all-in-one manner, consequently integrating originally separate terminal applications. Therefore, customer-oriented versatility is one of the core targets for reconfigurable technology. Second, achieving the virtually infinite reutilization of hardware resources at a restricted timescale is of critical concern for reconfigurable hardware schemes. Reconfigurable neuromorphic hardware platforms can be viewed as an aggregation of reprogrammable components, subsequently bringing about efficient temporal reuse, hardware simplification, and scalability. Last but not least, noninvasive and reproducible switch between different patterns should be highlighted, motivating a more intensive research interests and widespread commercial implementations of brain-inspired devices.

The development of reconfigurable neuromorphic computing is still in its fancy. Although prior studies have devoted great efforts at the material and device level, the critical parameters such as robustness, cycling endurance, variability, and intrinsic stochasticity still urge for further improvements. First, the unreliable driving mechanisms (e.g., magnetic soliton's dynamics, charge trapping, ferroelectric polarization, and so on) might accumulate the irreversible structure change which degrade the reproducibility. Second, a great sense of research is restricted to synaptic devices and only realize the collection of different plastic response which present poor application-level implementations. Additionally, reconfigurable neuromorphic devices also face unignorable cycle-to-cycle variability and device-to-device

nonuniformity, which hinder the development of reconfigurability, and more research on the materials and device architecture should be conducted. Multi-paradigm switching of neuronic and synaptic functions in a single device seems to be a successful case,[310] but the existent studies are unable to mimic the relatively comprehensive biologic characteristics of neither synapses nor neurons. Although reconfigurable hardware implementation of neuromorphic computing is a hot-button issue appealing to researchers, successfully integrated computing primitives or achievable functional paradigms are still limited, which calls for further investigations.

In our review, state-of-art progresses from different hierarchies has been highlighted. For reconfigurable neuromorphic computing at the material and device level, we have reviewed the comprehensive mechanisms including ion dynamics, carrier migration, phase transition, spintronics, and photonics. Depending on these modulating mechanisms, various brain-like functions can be integrated at the unit-cell level, which requires elaborate material engineering and device configurations. We introduce the representative achievements in enhancing the reconfigurability of neuromorphic electronics, for example, multiplasticity for synaptic devices, hybrid neural and synaptic functions, reconfigurable Boolean logic functions for efficient neural networks and general-purposed neural network accelerators. Particularly, the reconfigurable filament dynamics driven by electrochemical metallization or valance change endow the neuromorphic devices abundant freedoms to choose between volatile TS mode and nonvolatile RS mode by simply changing external optical or electric input, which originally requires a more complex circuit configuration. Compact integrated Boolean logic functions for neural networks have been successfully reported with reconfigurable neuromorphic devices. For instance, by utilizing spintronic mechanisms such as magnetic texture, spin-orbit torque, artificial spin ice, and so on, a complete set of in-memory logics can be achieved and subsequently used for more efficient neural algorithms surpassing the conventional CMOS.

For reconfigurable neuromorphic computing at the integration level, the improvement of inherent programmability is considered from two main technologies, namely, CMOS- and ReRAM-based routines. Specifically, the reconfigurable heterogeneous integration technology employs the flexible optical interlayer connection cooperating with stackable chip layers rather than traditional complex hardwire strategy and unalterable chip design, significantly enhancing the freedom degree of hierarchical and multidomain network topologies. Benefiting from closely mimicking the cerebral cortex, SNN-oriented integration schemes provide an event-based working mechanism and intrinsic fault-tolerant granularity, which bring about rich spatiotemporal dynamics, area and energy efficiency, and anti-interference properties. ANN-oriented approaches feature data-intensive computing and exact equivalence, leading to higher energy consumption and resource requirements. It should be noted that, although SNNs possess more brain-like characteristics, the ANN-based strategies provide better technological maturity, popularization, and compatibility with silicon-based CMOS technology. Therefore, exploring which is the most appropriate fashion and balancing the advantages and drawbacks between these two paradigms, are of crucial importance for researchers to concern.

Reconfigurability in neuromorphic hardware promise to be game-changing for deeper artificial intelligence in the post-Moore era. The future challenging obstacles and opportunities can be foreseen as follows:

i. More powerful functional integration: Abundant functional modules are critical for reconfigurable neuromorphic devices to tackle real-world scenarios. Although a variety of implementations are being explored for reconfigurable neuromorphic computing, the number of current achievable functions is restricted, and more comprehensive synthesis of brain-inspired components remain exclusive.
ii. Robust switch: Pursuing highly reproducible and stable switches are fundamental in reconfigurable neuromorphic devices. However, the limited endurance and retention performances, as well as huge cycling capability difference between different paradigms severely hamper the improvement of overall switching robustness.
iii. Self-adaptive capability: Grow-when-required neuromorphic hardware platforms, featuring self-adaptive capability, are of essential importance for next-generation artificial intelligence to perform on-demand practical tasks in ever-changing circumstances.

Ultimately, the multidisciplinary efforts spanning mechanisms, materials, devices, and integrations are necessary to expedite the prosperity of reconfigurable neuromorphic computing. A wide variety of practical applications of reconfigurable neuromorphic devices can be anticipated which present enormous potential to dominate the next wave of AI revolution.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

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